14.1 A 0.004mm² 250µW ΔΣ TDC with Time-Difference Accumulator and a 0.012mm² 2.5mW Bang-Bang Digital PLL Using PRNG for Low-Power SoC Applications

Jong-Phil Hong, Sung-Jin Kim, Jenlung Liu, Nan Xing,
Tae-Kwang Jang, Jaejin Park, Jihyun Kim, Taeik Kim, Hojin Park

Samsung Electronics, Yongin, Korea

As digital CMOS technology scales to 32nm and below, small and low-voltage clock and timing generators are in high demand to avoid complex analog operations and to meet stringent phase noise requirements. There have been several approaches to convert analog systems to their digital counterparts and a high-resolution time-to-digital converter (TDC) is a key element for the digitalization of analog circuits (Fig. 14.1.1). Recently, TDCs using a noise shaping technique with oversampling have been introduced to improve resolution [1]. However, they tend to be power hungry or require analog-intensive circuitry as they convert signals from the time domain to the voltage domain in order to perform arithmetic operations. A digital PLL (DPLL) is another crucial SoC component, and low-power area-efficient DPLLs are challenging to design. This paper presents a time-domain low-power ΔΣ TDC with a time-difference accumulator and an area-efficient, low-power, and fast-lock DPLL composed of a synthesizable bang-bang phase and frequency detector (BB-PFD), with a gain boosting mode and a pseudo-random number generator (PRNG).

The proposed first-order ΔΣ TDC is composed of a single-bit time-domain quantizer, a time-difference accumulator, two delay elements and MUXs, as shown in Fig. 14.1.2 (a). The time-difference accumulator can be implemented by two time-difference adders (TDAs) (see Fig. 14.1.2 (a)). The output of each TDA feeds the input of the other TDA. Since an identity of the proposed time difference addition (zero time difference) is an input operand to TDA_2, TDA_2 operates as a unit-gain "time difference register", which is identical to the z^{-1} function in a discrete-time system. By taking IN_A and $\overline{IN_A}$ as the *AWK* inputs of TDA_2 and TDA_1, respectively, a sequence of input time differences can be accumulated. The digital-to-time conversion in the feedback path and the residue operation of the ΔΣ loop are performed by multiplexing the input edges corresponding to the previous output sample.

The TDA in Fig. 14.1.2 (b) is composed of two gated delay-buffer (GDB) cells [2]. The two inverters of each GDB are cascaded with a load capacitor, C_{mid}. The first inverters, denoted as GI, have two additional control inputs, *HLD* and *AWK*. If a rising edge appears on *HLD*, the power supply and ground are disconnected from the GI until another rise edge appears on *AWK*. Input edges to the GDB cell, for which the time difference is represented as ΔT_{IN}, are asserted through two ports, *IN* and *HLD*. After a first edge is applied to *IN*, the intermediate voltage, V_{mid}, starts to be discharged toward ground and then, V_{mid} is held steady when a second edge is applied to *HLD*. In the middle of the hold state, a trigger edge resumes the discharging. Then, a rising edge is eventually generated at the output port, *OUT*, when the trigger edge is applied to *AWK* at an arbitrary time instant to wake up GDB. The time difference between *AWK* and *OUT* is the residual time of the input time difference from T_d (i.e., $T_{OUT}-T_{AWK}=T_d-\Delta T_{IN}$). In other words, the input time difference, ΔT_{IN}, is temporarily stored and its inverse ($-\Delta T_{IN}$) can be sampled at an arbitrary time instant with a constant offset. Offset delays (T_{off}), asserted to each GDB, make the input positive time differences, ΔT^*_{IN1} and ΔT^*_{IN2}, respectively. Note that the cross-connected input for the second operand of the TDA makes the input time difference its inverse element. As a result, two bipolar time differences can be accumulated by the TDA ($\Delta T_{OUT}=T_{OUT2}-T_{OUT1}=(T_d-\Delta T^*_{IN2})-(T_d-\Delta T^*_{IN1}) =\Delta T_{IN1}+\Delta T_{IN2}$).

Figure 14.1.3 (a) shows the proposed BB-PFD DPLL. The DCO depicted in Fig. 14.1.3 (a) consists of a 4-stage differential ring oscillator and switched-controlled capacitance bank arrays that have 4b binary-weighted coarse tuning, and 256b thermometer-coded fine tuning, controlled by automatic frequency control (AFC) and row/column controllers (Row/Col), respectively. Since the coarse tuning arrays significantly reduce the burden of the fine tuning operation range, the DCO achieves lower power consumption, better frequency resolution, and faster lock time.

In the case where a high-order MASH ΔΣM is applied to the ring-DCO-based DPLL with poor frequency resolution due to the wide frequency tuning range, high-frequency noise in the ΔΣM degrades the natural phase noise of the DCO, resulting in high period jitter. Moreover, a wide-dithering range in a high-order MASH ΔΣM increases deterministic jitter. In the proposed DPLL, the accumulator improves effective frequency resolution with only 1b fractional dithering and the PRNG suppresses spurious tones generated by periodic error in the accumulator. Since the dithering range is narrower and high-frequency noise is smaller than those of the high order MASH ΔΣM, the period and deterministic jitter of the proposed DPLL are both smaller. The accumulator output signals can be randomized further by using the dithered dual-modulus counter (8/9) output for the sampling clock signal to the accumulator and PRNG. The proposed PRNG in Fig. 14.1.3 (b) consists of Galois linear-feedback shift registers (LFSRs), comparators, D flip-flops, and MUXs. The total number of output bit sequences of the LFSRs increases from 2^n-1 to $2\cdot(2^n-1)$, as shown in Fig. 14.1.3 (b). The proposed PRNG makes the total number of 1s and -1s in the sequence even, which keeps the time-averaged value of the accumulator output the same as the normalized fractional input bits. The spurious tones of the accumulator output are suppressed through the 6b randomized fractional input values by the proposed PRNG. The BB-PFD-based DPLL has been designed with a small loop gain to suppress the limited-cycle effect, however, the small loop gain results in a longer lock time. The proposed DPLL effectively reduces the lock time using AFC, and a newly-introduced BB-PFD with a gain-boosting circuit. AFC initially selects a DCO coarse tuning code to the target frequency and then, the BB-PFD starts a fine-locking process. The synthesizable PFD shown in Fig. 14.1.4 consists of a core bang-bang PFD, which generates an UP/DN signal by comparing FREF with FEED, a high-gain mode selector that is enabled when FEED is earlier than E_FREF or later than L_FREF, and an asynchronous reset block which generates a reset pulse, A_RESET.

The proposed TDC and DPLL are fabricated in a 32nm CMOS process and the active area of the TDC and the DPLL occupy 0.004 and 0.012mm², respectively. The measured power dissipation of the TDC is 250µW for a 10MS/s input signal. The current consumption of the DPLL is 3mA with a 0.85V supply voltage at 1.5GHz. In order to measure the performance of the TDC, a time-difference input sequence is applied to the TDC by differential voltage-controlled delay lines (VCDLs). Figure 14.1.5 shows a 65,536 point FFT of the TDC output with a Hanning window for a 100kHz single-tone input of $100ps_{pp}$, and also shows a performance comparison with other TDCs. Noise-shaping of 20dB/decade is clearly evident at high frequency with flicker noise dominant at low frequency. The measured SNDR is 28.95dB, with integrated noise from 1kHz to 100kHz. Measured lock time (25µs) with AFC and a high gain of 16 is approximately 9 times faster than without high-gain mode (220µs). The measured period RMS and peak-to-peak jitter are 13.5ps and 70.9ps under the same conditions, respectively. The measured phase noise plot in Fig. 14.1.6 illustrates that the proposed DPLL effectively suppresses the fractional dithering spur at 13MHz offset from -95dBc/Hz to -102dBc/Hz without degrading DCO phase noise compared to 2nd and 3rd-order ΔΣMs. A performance comparison of the DPLL is summarized in Fig. 14.1.6 and the chip micrograph of both TDC and DPLL is shown in Fig. 14.1.7.

References :

[1] Y. Cao, et al., "A 1.7mW 11b 1-1-1 MESH ΔΣ Time-to-Digital Converter," *ISSCC Dig. Tech. Papers,* pp. 480–481, 2011.

[2] S.J. Kim, "*Time Domain Algebraic Operation Circuits for High Performance Mixed-Mode System*," *MS Thesis*, KAIST, 2010.

[3] M.Z. Straayer, et al., "An efficient high-resolution 11-bit noise-shaping multipath gated ring oscillator TDC," *IEEE Symp. VLSI Circuits,* pp. 82-83, 2008.

[4] A. Rylyakov, et al., "Bang-Bang Digital PLLs at 11 and 20GHz with sub-200fs Integrated Jitter for High-Speed Serial Communication Applications," *ISSCC Dig. Tech. Papers*, pp. 94-95, 2009.

[5] M. Chen, et al., "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," *ISSCC Dig. Tech. Papers*, pp. 472-473, 2010.

 978-1-4673-0377-4/12/$31.00

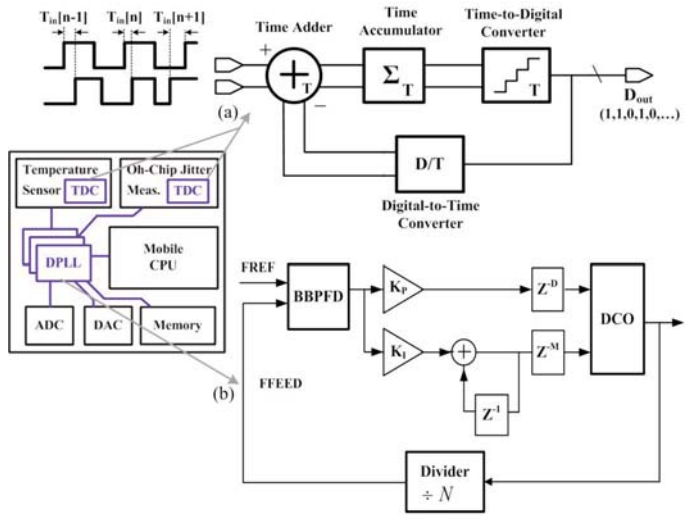


Figure 14.1.1: Block diagram of a classic SoC platform. (a) ΔΣ TDC and (b) digital PLL.

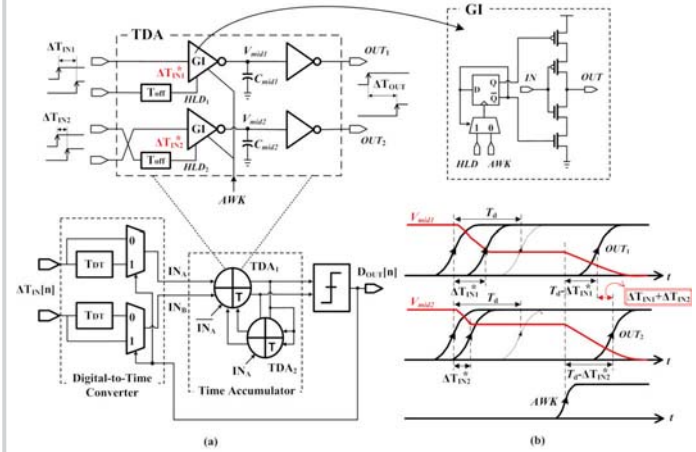


Figure 14.1.2: (a) Schematic of the proposed ΔΣ TDC and (b) operation principle of the TDA.

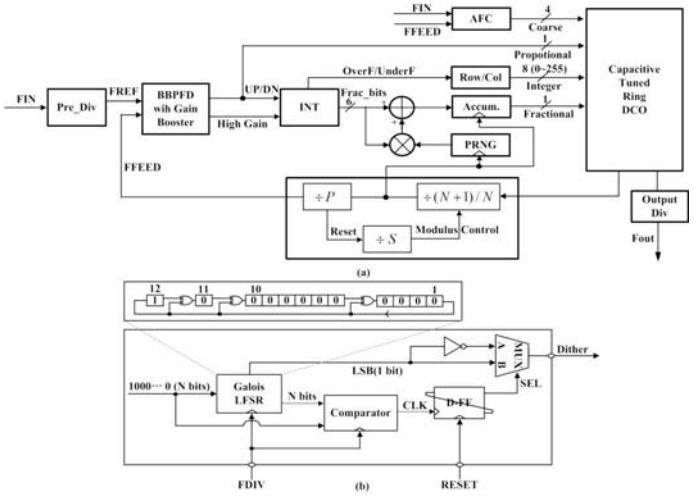


Figure 14.1.3: Block diagram of the proposed (a) digital PLL and (b) PRNG using Galois linear feedback shift registers (LFSRs).

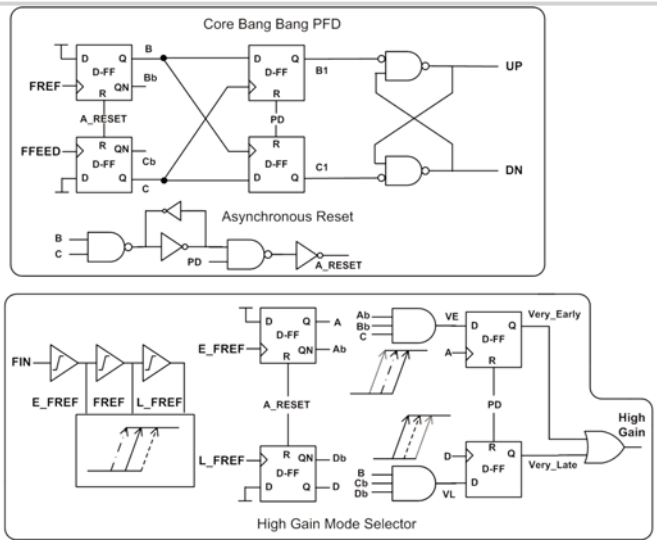
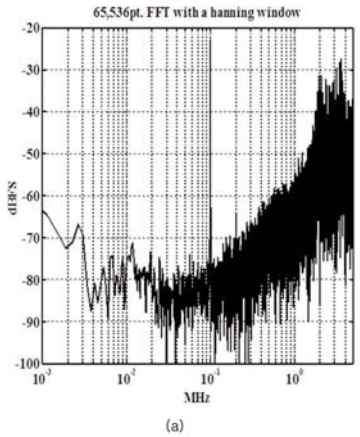


Figure 14.1.4: Schematic and operating behavior of the synthesizable bang-bang PFD with a gain boosting circuit.

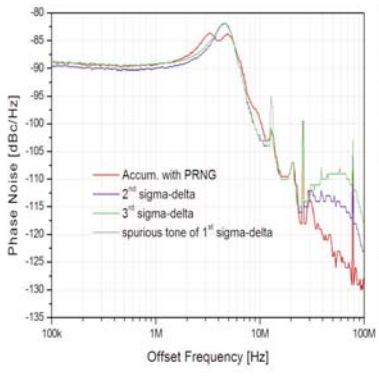


(a)

	[1]	[3]	This work
Technology (nm)	130	130	32
Supply (V)	1.2	1.5	1.0
Area (mm^2)	0.11	0.04	0.004
Power (mW)	1.7 @50MS/s	2.2-21 @50MS/s	0.25 @10MS/s
Bandwidth (Hz)	100k	1M	100k
Oversampling ratio	250	25	50
Effective resolution (ps)	10.5	1.2	4.4

(b)

Figure 14.1.5: (a) Measured ΔΣ TDC output for a $100ps_{pp}$, 100kHz input sequence and performance comparison.



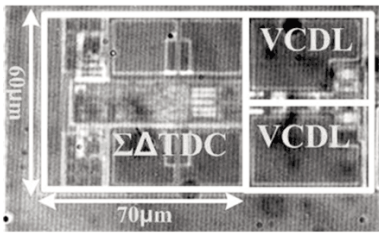
(a)

	[4]	[5]	This work
Technology (nm)	65	65	32
Area (mm^2)	0.048	0.027	0.012
Power (mW)	19.7 @2GHz	3.4 @800MHz	2.5 @1.5GHz
PLL Frequency (GHz)	0.5 – 4.4	0.6 – 0.8	0.7 – 1.8
Phase Noise@1MHz offset (dBc/Hz)	-80 at 2GHz	-98 at 400MHz	-89 at 1.5GHz
RMS Jitter (ps)	1.1 @2.06GHz	21.5 @400MHz	13.5 @46.875MHz 1.45@1.5GHz

(b)

Figure 14.1.6: (a) Measured phase noise plots, for 2nd, 3rd order ΔΣM, and accumulator with PRNG (FREF=26MHz, FOUT=1.274MHz), and (b) performance comparison.

14



(a)

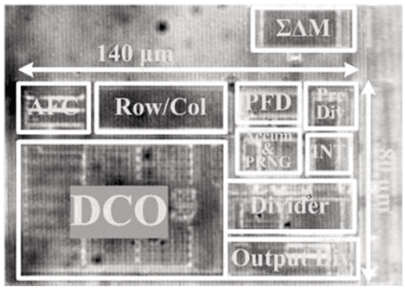


Figure 14.1.7: Chip micrograph of the proposed (a) ΔΣ TDC and (b) BB-PFD DPLL.

978-1-4673-0377-4/12/$31.00