Intergrated Circuits report 4

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4.1

Derive the switching probabilities in Table

TABLE Switching probabilities

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \bar{P}_A \bar{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\bar{P}_A \bar{P}_B$
XOR2	$P_A \bar{P}_B + \bar{P}_A P_B$

4.5

You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 450 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm^2 and runs at 450 MHz at $V_{DD} = 0.9$ V.

8.1

Design a fast 6-input OR gate in each of the following circuit families. Sketch an implementation using two stages of logic (e.g., NOR6 + INV, NOR3 + NAND2, etc.). Label each gate with the width of the pMOS and nMOS transistors. Each input can drive no more than 30 λ of transistor width. The output must drive a 60/30 inverter (i.e., an inverter with a 60 λ wide pMOS and 30 λ wide nMOS transistor). Use logical effort to choose the topology and size for least average delay. Estimate this delay using logical effort. When estimating parasitic delays, count only the diffusion capacitance on the output node.

a) static CMOS
b) pseudo-nMOS with pMOS transistors 1/4 the strength of the pulldown stack
c) domino (a footed dynamic gate followed by a HI-skew inverter); only optimize the delay from rising input to rising output

8.18

Sketch pseudo-nMOS 3-input NAND and NOR gates. Label the transistor widths. What are the rising, falling, and average logical efforts of each gate?

8.19

Sketch a pseudo-nMOS gate that implements the function

$$F = \overline{A(B+C+D) + E \cdot F \cdot G}$$

8.27

Sketch dynamic footed and unfooted 3-input NAND and NOR gates. Label the transistor widths. What is the logical effort of each gate?

8.39

Sketch 3-input XOR functions using each of the following circuit techniques:

a) Static CMOS

b) Pseudo-nMOS

c) Dual-rail domino

9.4

Sketch a pseudo-nMOS gate that implements the function

$$F = \overline{A(B+C+D)+E\cdot F\cdot G}$$

9.10

Consider a flip-flop built from a pair of transparent latches using nonoverlapping clocks. Express the setup time, hold time, and clock-to-Q delay of the flip-flop in terms of the latch timing parameters and $t_{\text{nonoverlap}}$, relative to the rising edge of ϕ_1.

9.12

Determine the minimum clock period at which the circuit in Figure 10.55 will operate correctly for each of the following logic delays. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay

a) $\Delta 1 = 300$ ps; $\Delta 2 = 400$ ps; $\Delta 3 = 200$ ps; $\Delta 4 = 350$ ps

b) $\Delta 1 = 300$ ps; $\Delta 2 = 400$ ps; $\Delta 3 = 400$ ps; $\Delta 4 = 550$ ps

c) $\Delta 1 = 300$ ps; $\Delta 2 = 900$ ps; $\Delta 3 = 200$ ps; $\Delta 4 = 350$ ps