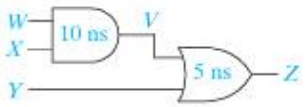
Digital Engineering 3rd report

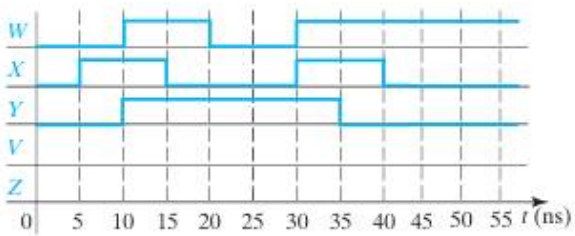
● **제출 : 5월 26일(월) 수업시간**

● **디지털 공학 과제 주의사항**

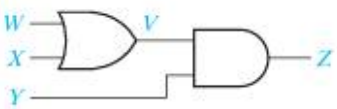
1. 과제는 반드시 **자필**로 작성하셔야 합니다.
2. **문제 풀이 과정**이 다 들어가 있어야 하며, 답에는 반드시 **밑줄이나 박스** 등의 답을 알아볼 수 있는 표기 바랍니다.
3. **A4용지**에 반드시 **학번 이름**을 포함하여 제출 바랍니다.
4. 문제는 **7판 원서** 기준으로 출제되었습니다.
5. 스테이플러는 종이 **왼쪽**에 찍어주시기 바랍니다.
6. 문제의 순서가 명확하도록 **페이지 번호** 표기바랍니다.
7. 풀이과정을 알아볼 수 없는 경우 불이익이 발생할 수 있습니다.

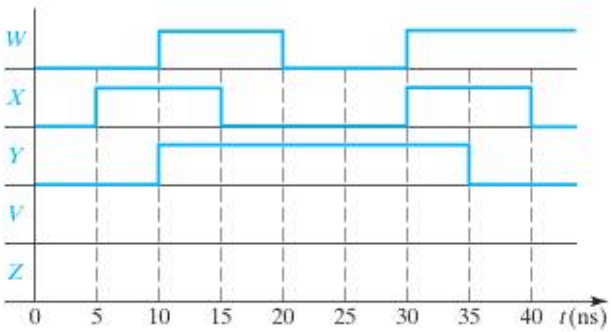
8.10 Draw the timing diagram for V and Z for the circuit. Assume that the AND gate has a delay of 10 ns and the OR gate has a delay of 5 ns.





8.12 Complete the timing diagram for the given circuit. Assume that both gates have a propagation delay of 5 ns.



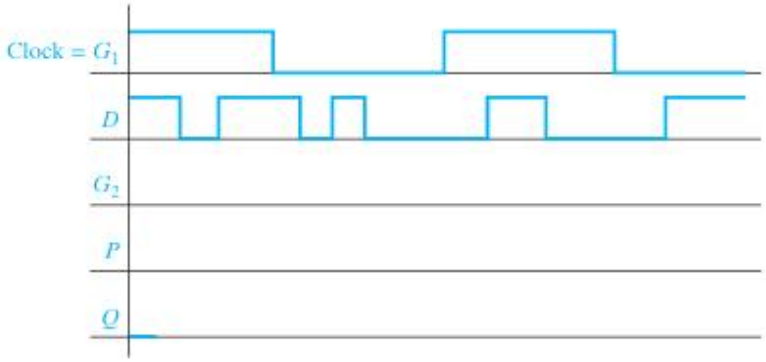


9.7 An adder for Gray-coded-decimal digits (see Table 1-2) is to be designed using a ROM. The adder should add two Gray-coded digits and give the Gray-coded sum and a carry. For example, 1011 + 1010 = 0010 with a carry of 1 (7 + 6 = 13). Draw a block diagram showing the required ROM inputs and outputs. What size ROM is required? Indicate how the truth table for the ROM would be specified by giving some typical rows.

9.25 Show how to make an 8-to-1 MUX using two 4-to-1 MUXes, two three-state buffers, and one inverter.

11.4 Design a gated D latch using only NAND gates and one inverter.

11.5 What change must be made to Figure 11-19(a) to implement a falling-edge-triggered D flip-flop? Complete the following timing diagram for the modified flip-flop.



11.11 Complete the following timing diagram for an S-R latch. Assume Q begins at 1.