Digital engineering 4th report

* 제출: 6월 18일(수) 기말고사 시작 전

* 디지털 공학 과제 주의사항

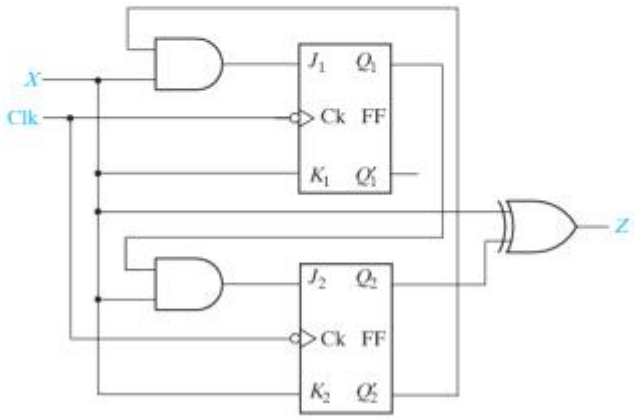
1. 과제는 반드시 **자필**로 작성하셔야 합니다.
2. **문제 풀이 과정**이 다 들어가 있어야 하며, 답에는 반드시 **밑줄이나 박스** 등의 답을 알아볼 수 있는 표기 바랍니다.
3. **A4용지**에 반드시 **학번 이름**을 포함하여 제출바랍니다.
4. 문제는 **7판 원서** 기준으로 출제되었습니다.
5. 스테이플러는 종이 **왼쪽**에 찍어주시기 바랍니다.
6. 문제의 순서가 명확하도록 **페이지 번호** 표기바랍니다.
7. 풀이과정을 알아볼 수 없는 경우 불이익이 발생할 수 있습니다.

12.8 Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . .
(a) Use J-K flip-flops.
(b) Use S-R flip-flops.
In each case, what will happen if the counter is started in state 000?

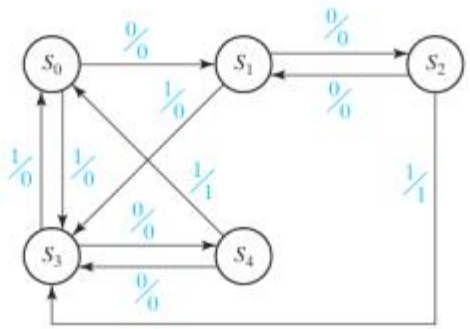
12.12 Design a left-shift register similar to that of Figure 12-10. Your register should shift left if $Sh = 1$, load if $Sh = 0$ and $L = 1$, and hold its state if $Sh = L = 0$.
(a) Draw the circuit using four D flip-flops and four 4-to-1 MUXes.
(b) Give the next-state equations for the flip-flops.

12.28 When started in state 0, an n-stage Johnson (twisted-ring) counter cycles through $2n$ states. Other count cycles will be obtained if the counter is started in other states. Determine all count cycles for the Johnson counter when
(a) $n = 3$,
(b) $n = 4$, and
(c) $n = 5$.

13.8 (a) Construct a transition table and state graph for the circuit shown.
(b) Construct a timing chart for the input sequence $X = 10101$. (Assume that initially $Q_1 = Q_2 = 0$ and that X changes midway between the rising and falling clock edges.) Indicate the times Z has the correct value.
(c) List the output values produced by the input sequence.



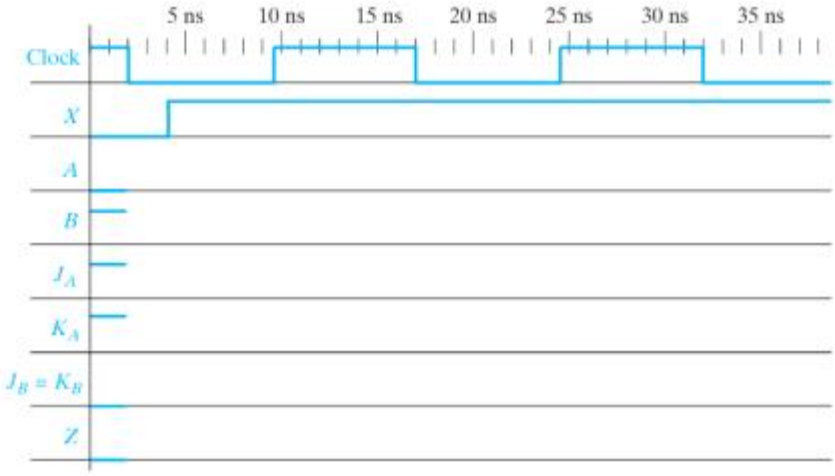
13.27 For the following state graph, construct a transition table. Then, give the timing diagram for the input sequence $X = 101001$. Assume X changes midway between the falling and rising edges of the clock, and that the flip-flops are falling-edge triggered. What is the correct output sequence?



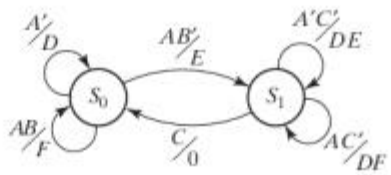
13.28 For the circuit of Problem 13.3, assume the delays of the NAND gates and NOR gates are 3 ns, and assume the delay of the inverter is 2 ns. Assume the propagation delays and setup times for the J-K flip-flops are 4 ns and 2 ns, respectively.

(a) Fill in the given timing diagram. The clock period is 15 ns, and 1-ns increments are marked on the clock signal. Does the circuit operate properly with these timing parameters?

(b) What is the minimum clock period for this circuit, if X is changed early enough? How late may X change with this clock period without causing improper operation of the circuit?



14.10 For the following state graph, construct the state table, and demonstrate that it is completely specified.



14.37 A sequential circuit has an input (X) and two outputs (S and V). X represents a 4-bit binary number N which is input least significant bit first. S represents a 4-bit binary number equal to $N + 2$, which is output least significant bit first. At the time the fourth input occurs, $V = 1$ if $N + 2$ is too large to be represented by four bits; otherwise, $V = 0$. The circuit always resets after the fourth bit of X is received. Find a Mealy state graph and table for the circuit.

Example: $X = 0111$ (binary 14 with the least significant bit first)
$S = 0000$ (because 14 + 2 = 16, and 16 requires 5 bits)
$V = 0001$

14.46 There are two errors in the state graph shown. One state is not completely specified for one combination of X_1 and X_2. In another state, there is a contradiction for one combination of X_1 and X_2. Correct the state graph by making two minor changes. Demonstrate that the modified state graph is completely specified.