
Integrated Circuits

Chapter 1: Introduction

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Course Administration

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❑ Text: *Integrated Circuit Design*, 4rd Ed.,
Revised Printing, Neil & David, ©2011

❑ Slides: <http://icat.cbnu.ac.kr>

❑ Grade:

Midterm Exam	~35%
Final Exam	~40%
Homeworks	~15%
Class participation	~10%

Introduction

- ❑ Integrated circuits: many transistors on one chip.
- ❑ Very Large Scale Integration (VLSI): bucketloads!
- ❑ Complementary Metal Oxide Semiconductor
 - Fast, cheap, low power transistors
- ❑ Today: How to build your own simple CMOS chip
 - CMOS transistors
 - Building logic gates from transistors
 - Transistor layout and fabrication
- ❑ Rest of the course: How to build a good CMOS chip

Lecture

1. Introduction CMOS Logic
2. MOS Transistor Theory
3. Nonideal Transistor Theory
4. DC & Transient Response
5. Logic Effort
6. Power
7. Sequential Circuit Design
8. Circuit Families
9. Scaling & Economics

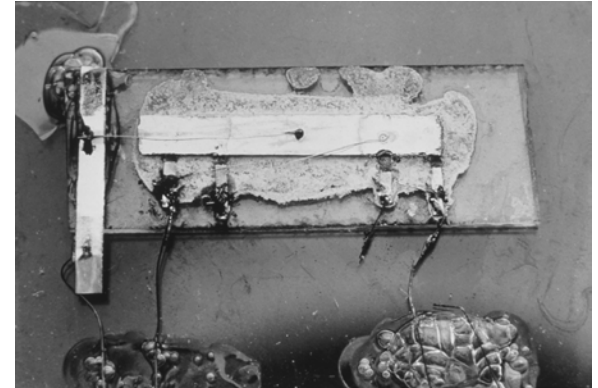
Outline

- ❑ A Brief History
- ❑ MOS Transistors
- ❑ CMOS Gate Design
- ❑ Pass Transistors
- ❑ CMOS Latches & Flip-Flops

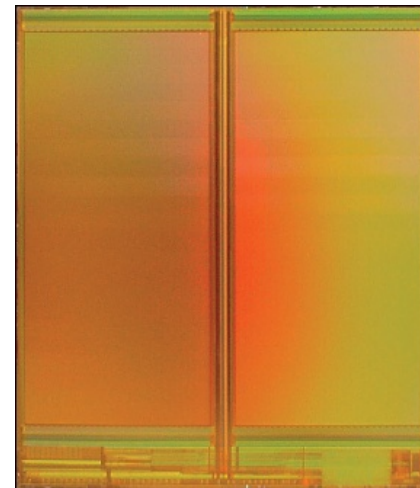
A Brief History

- ❑ 1958: First integrated circuit
 - Flip-flop using two transistors
 - Built by Jack Kilby at Texas Instruments

- ❑ 2010
 - Intel Core i7 μ processor
 - 2.3 billion transistors
 - 64 Gb Flash memory
 - > 16 billion transistors



Courtesy Texas Instruments



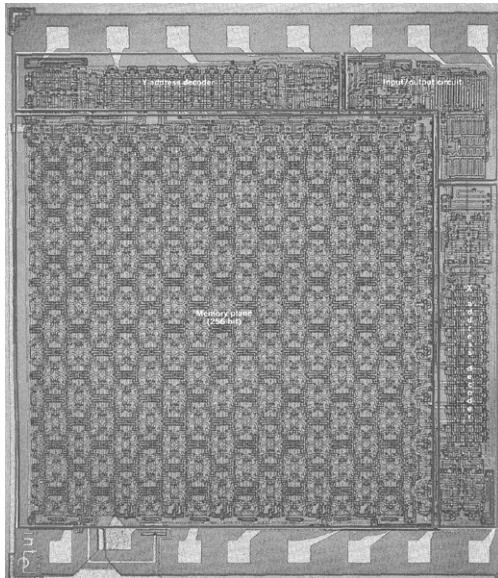
[Trinh09]
© 2009 IEEE.

Transistor Types

- ❑ Bipolar transistors
 - npn or pnp silicon structure
 - Small current into very thin base layer controls large currents between emitter and collector
 - Base currents limit integration density
- ❑ Metal Oxide Semiconductor Field Effect Transistors
 - nMOS and pMOS MOSFETS
 - Voltage applied to insulated gate controls current between source and drain
 - Low power allows very high integration

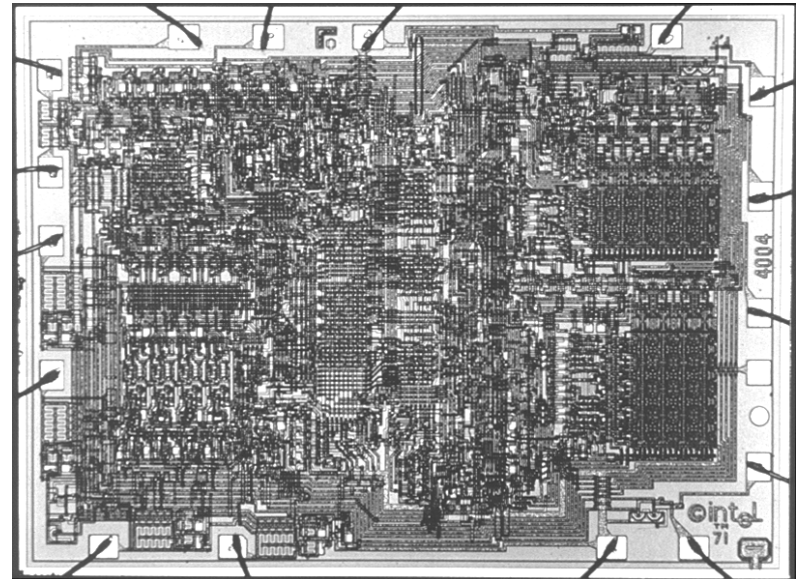
MOS Integrated Circuits

- ❑ 1970's processes usually had only nMOS transistors
 - Inexpensive, but consume power while idle



[Vadasz69]
© 1969 IEEE.

Intel 1101 256-bit SRAM



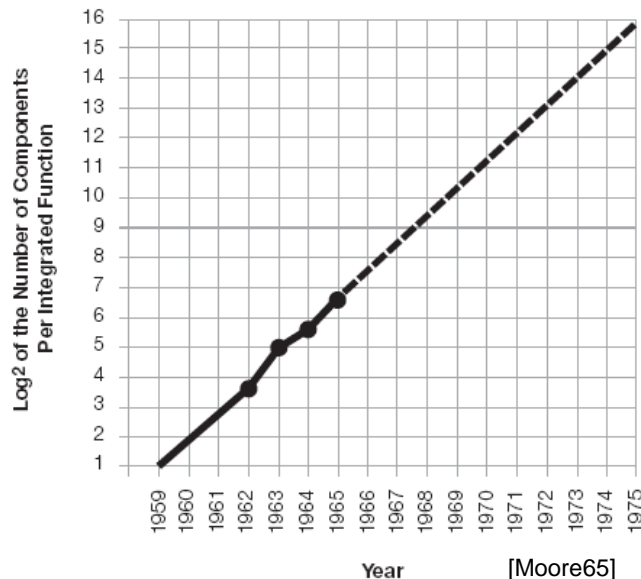
Intel
Museum.
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Intel 4004 4-bit μ Proc

- ❑ 1980s-present: CMOS processes for low idle power

Moore's Law: Then

- 1965: Gordon Moore plotted transistor on each chip
 - Fit straight line on semilog scale
 - Transistor counts have doubled every 26 months



[Moore65]
Electronics Magazine

Integration Levels

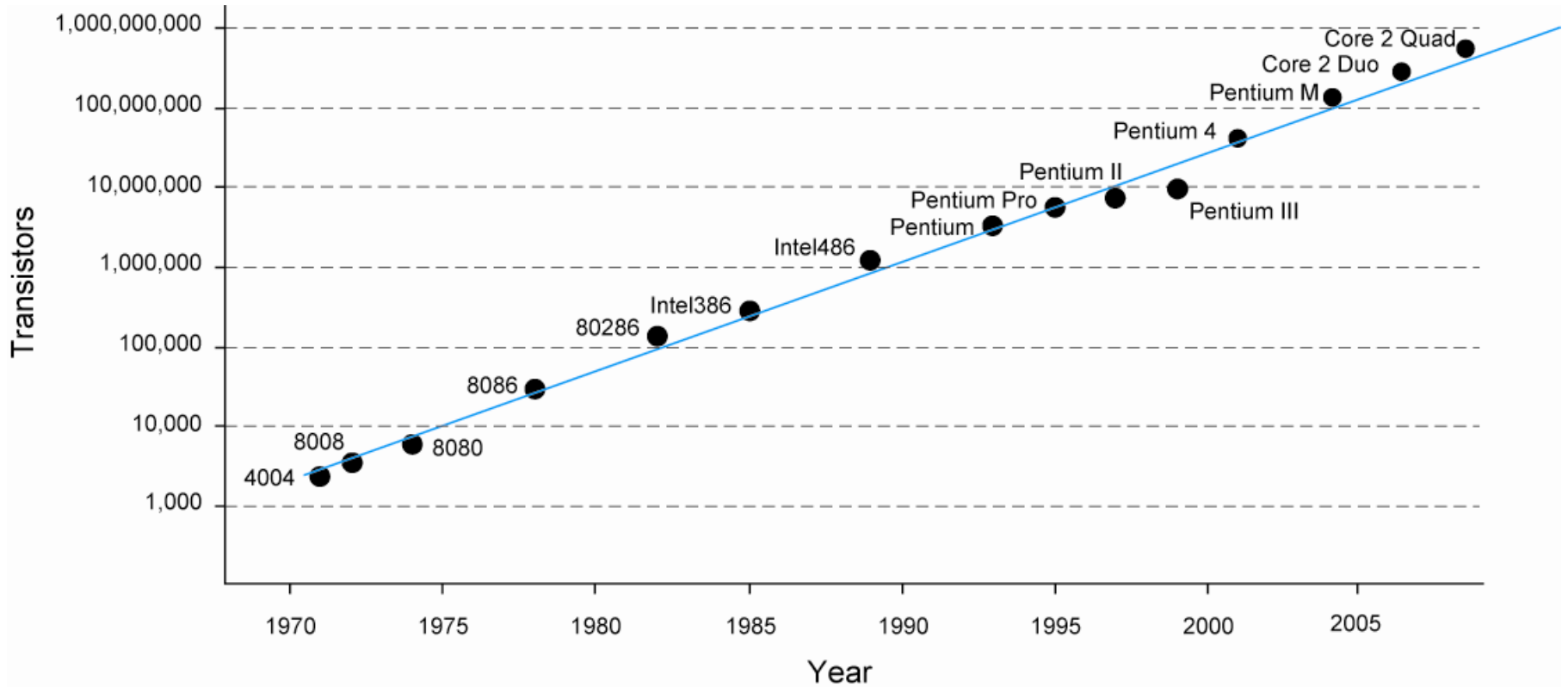
SSI: 10 gates

MSI: 1000 gates

LSI: 10,000 gates

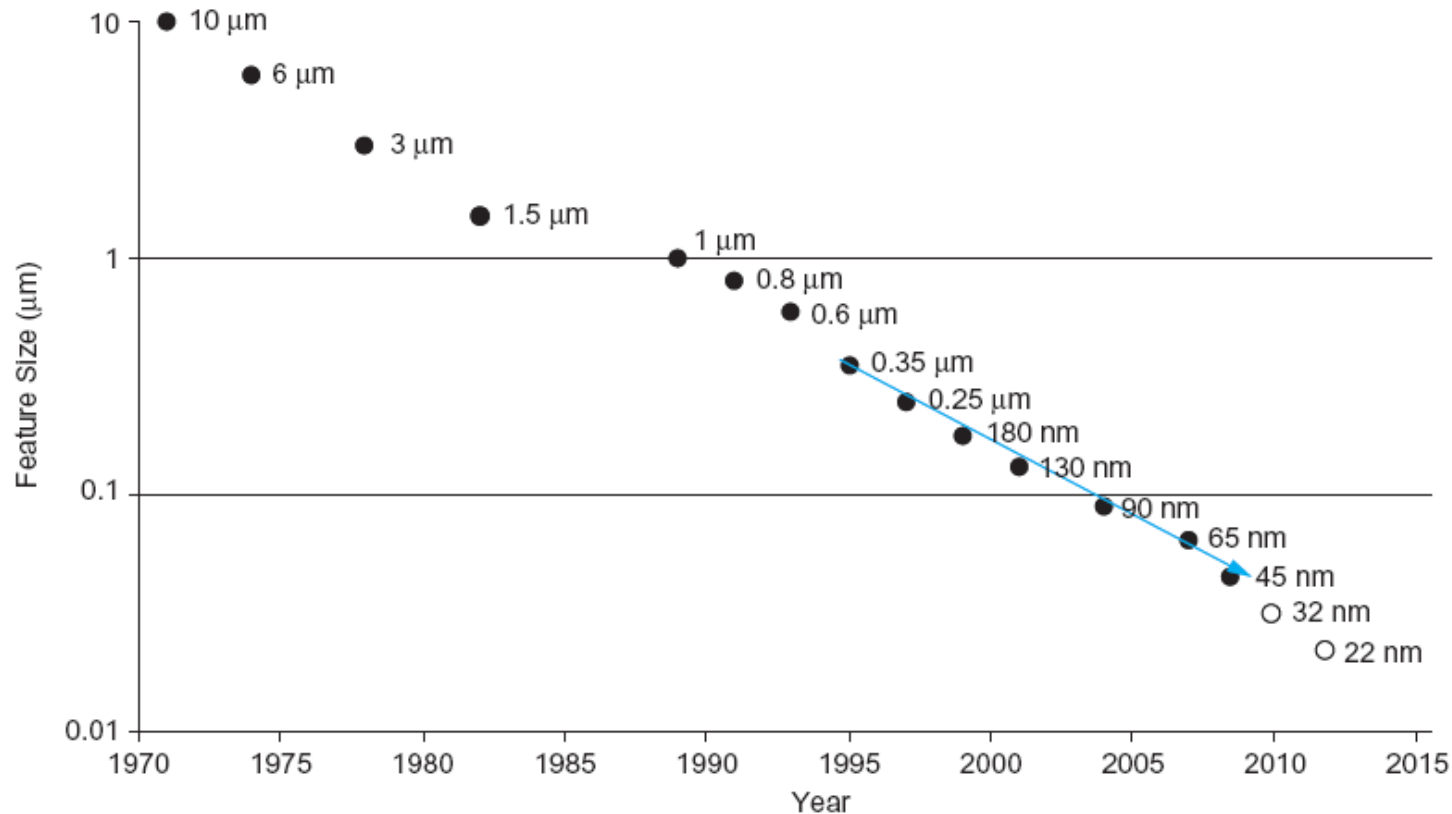
VLSI: > 10k gates

And Now...



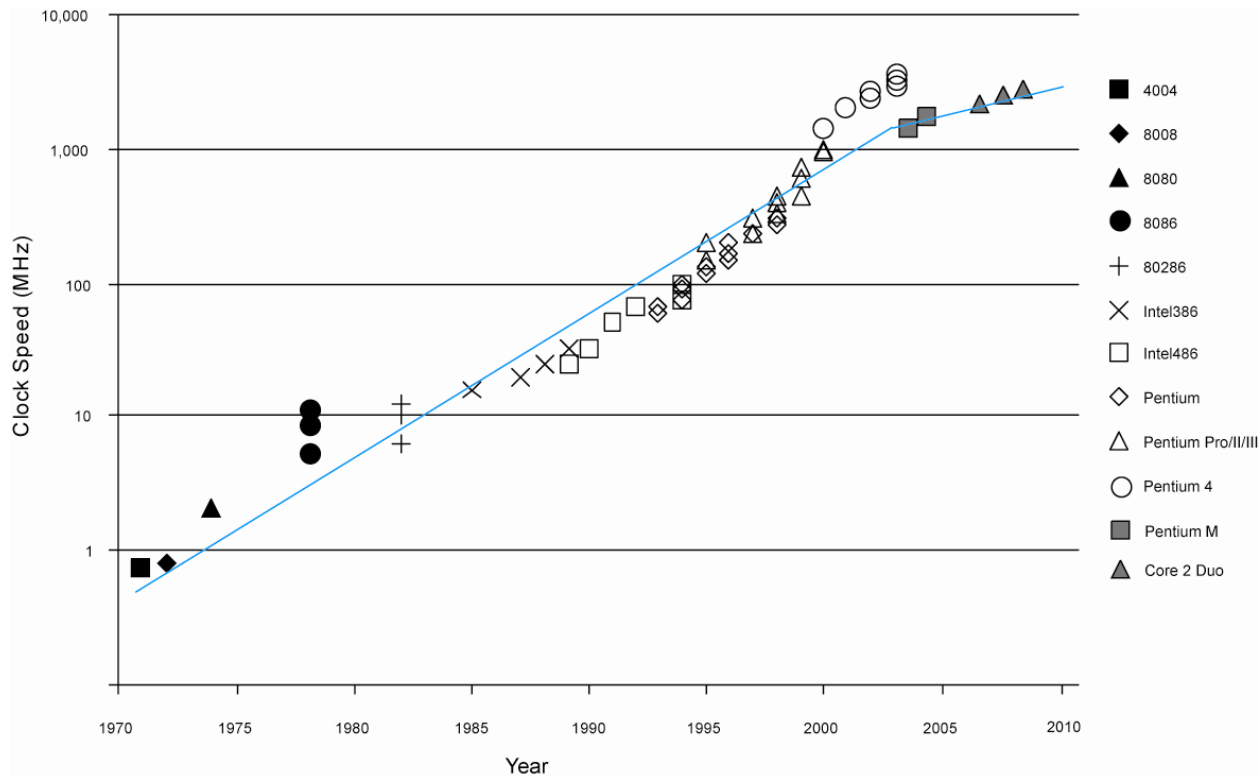
Feature Size

- Minimum feature size shrinking 30% every 2-3 years

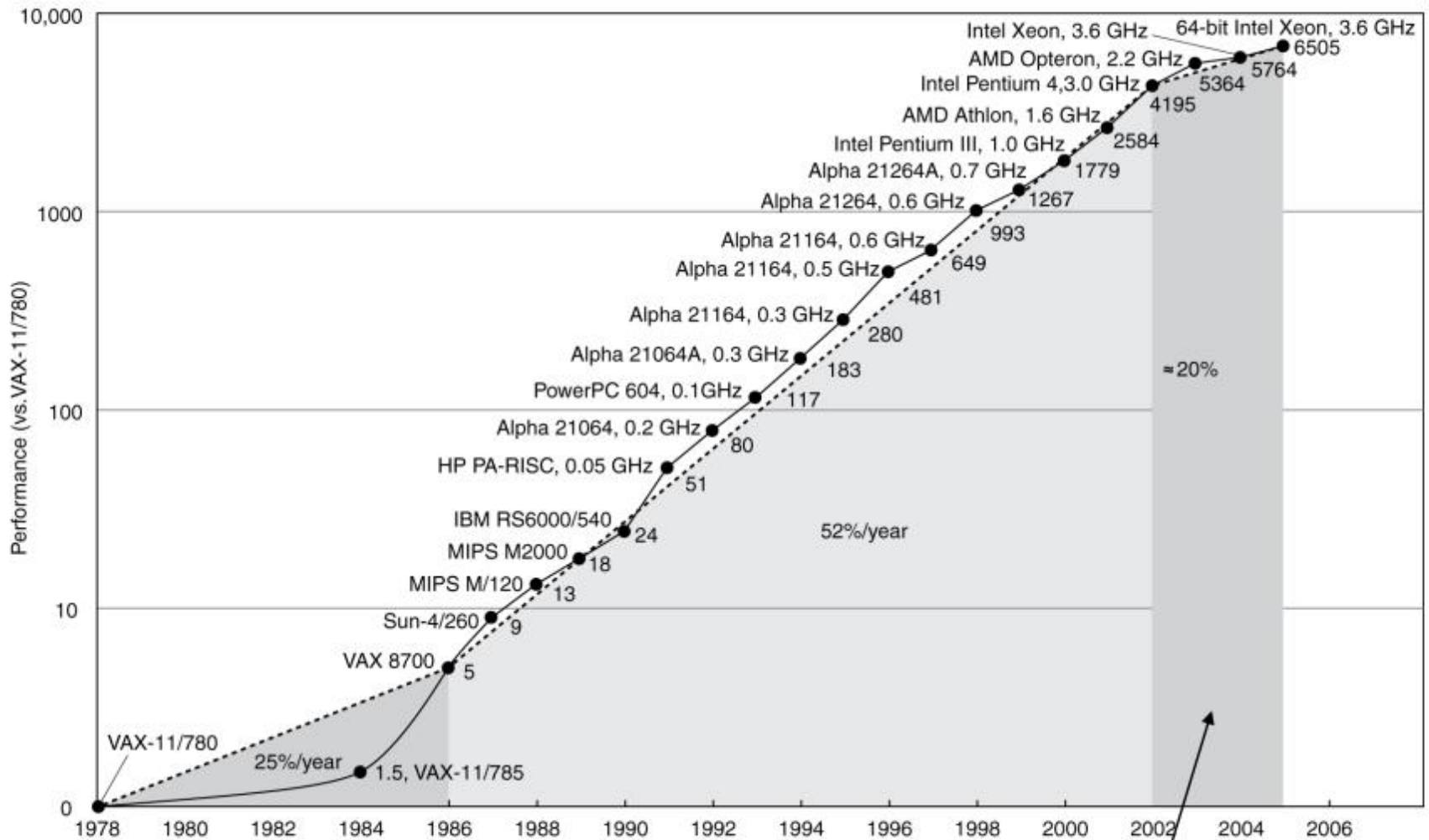


Corollaries

- Many other factors grow exponentially
 - Ex: clock frequency, processor performance



Uniprocessor Performance



Constrained by power, instruction-level parallelism, memory latency

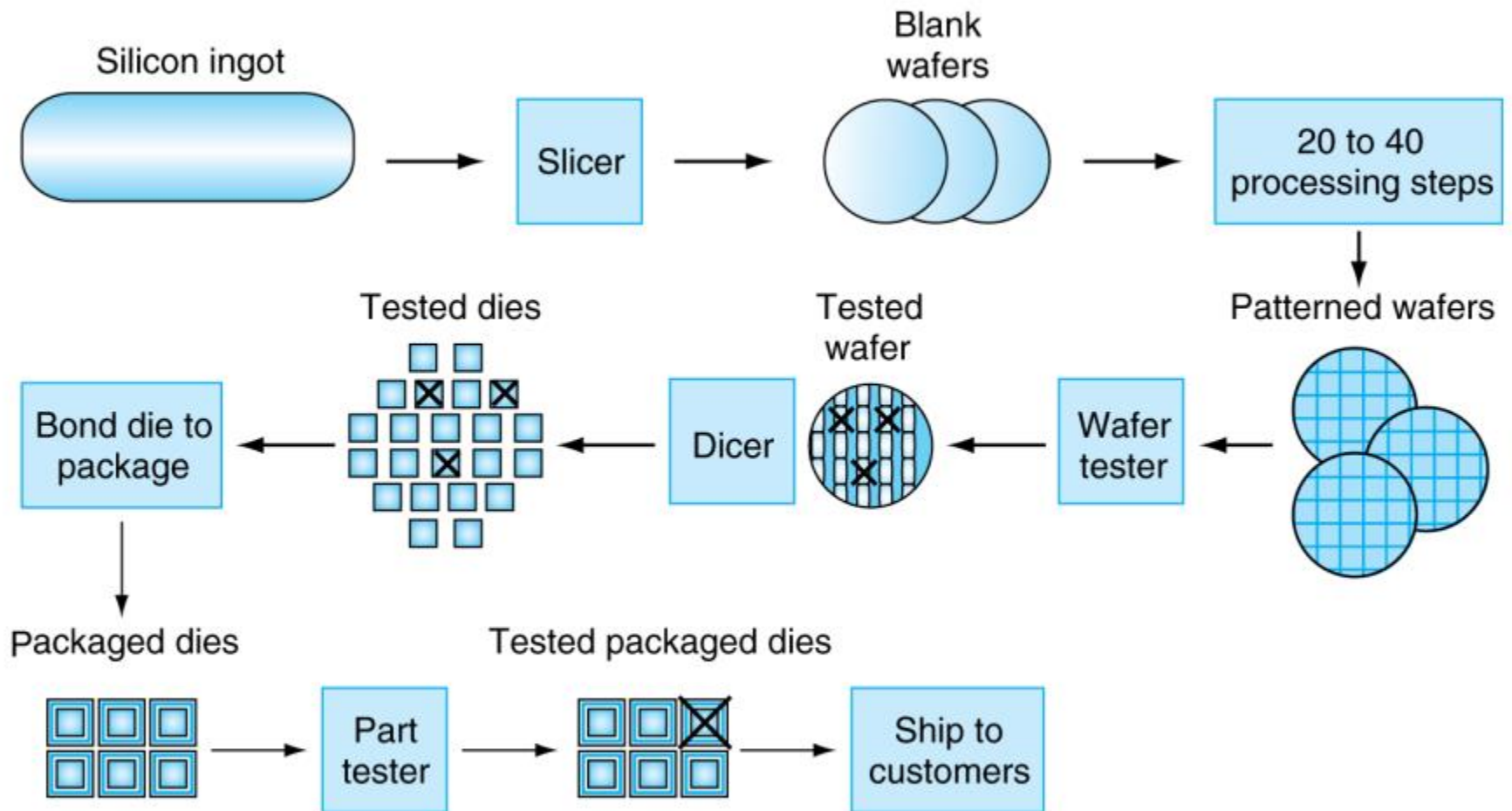
Multiprocessors

- The power challenge has forced a change in the design of microprocessors
- Multicore microprocessors
 - More than one processor per chip

Product	AMD Barcelona	Intel Nehalem	IBM Power 6	Sun Niagara 2
Cores per chip	4	4	2	8
Clock rate	2.5 GHz	~2.5 GHz?	4.7 GHz	1.4 GHz
Power	120 W	~100 W?	~100 W?	94 W

- Hard to do
 - Programming for performance
 - Load balancing
 - Optimizing communication and synchronization

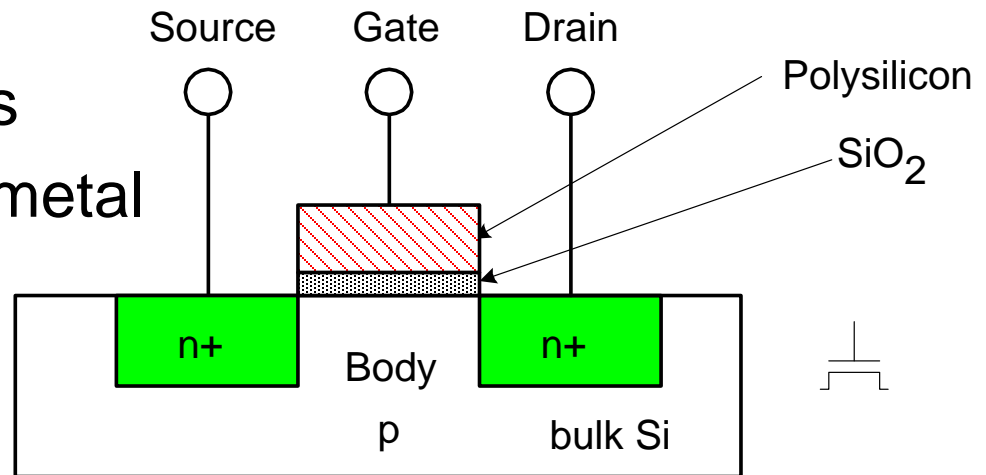
Manufacturing ICs



- **Yield**: proportion of working dies per wafer

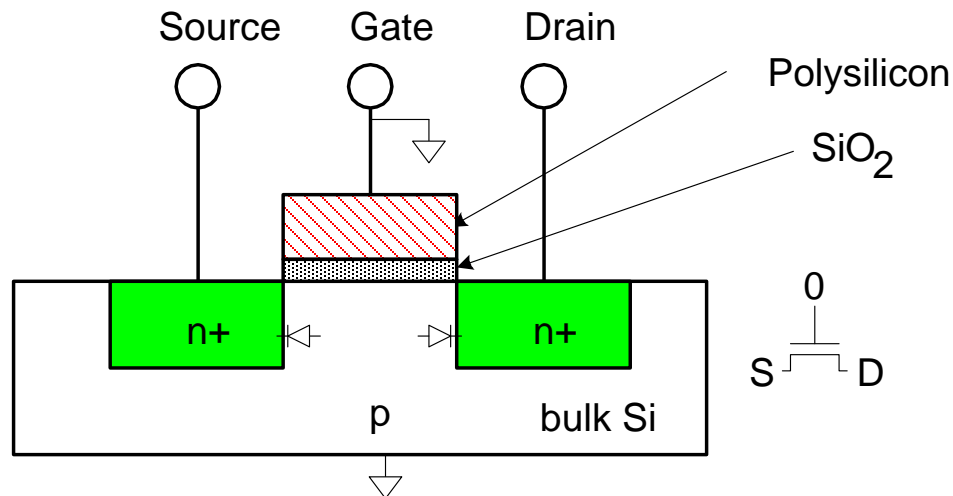
nMOS Transistor

- ❑ Four terminals: gate, source, drain, body
- ❑ Gate – oxide – body stack looks like a capacitor
 - Gate and body are conductors
 - SiO_2 (oxide) is a very good insulator
 - Called metal – oxide – semiconductor (MOS) capacitor
 - Even though gate is no longer made of metal



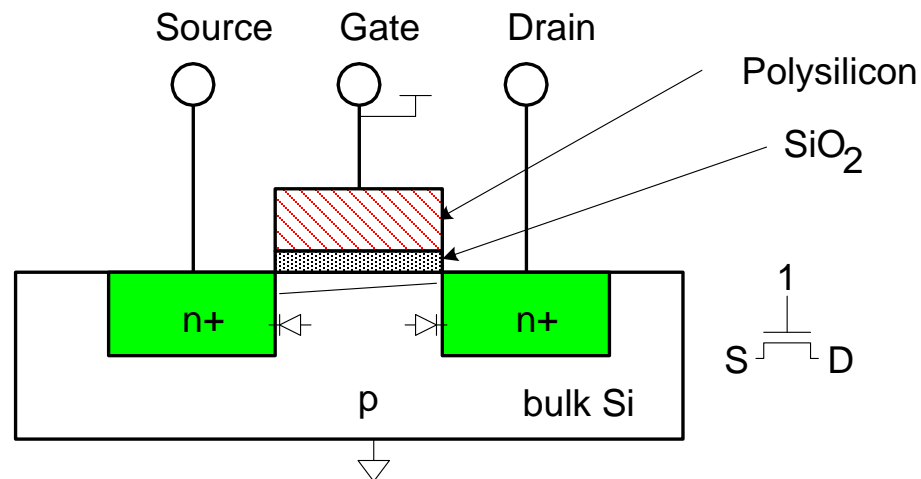
nMOS Operation

- ❑ Body is usually tied to ground (0 V)
- ❑ When the gate is at a low voltage:
 - P-type body is at low voltage
 - Source-body and drain-body diodes are OFF
 - No current flows, transistor is OFF



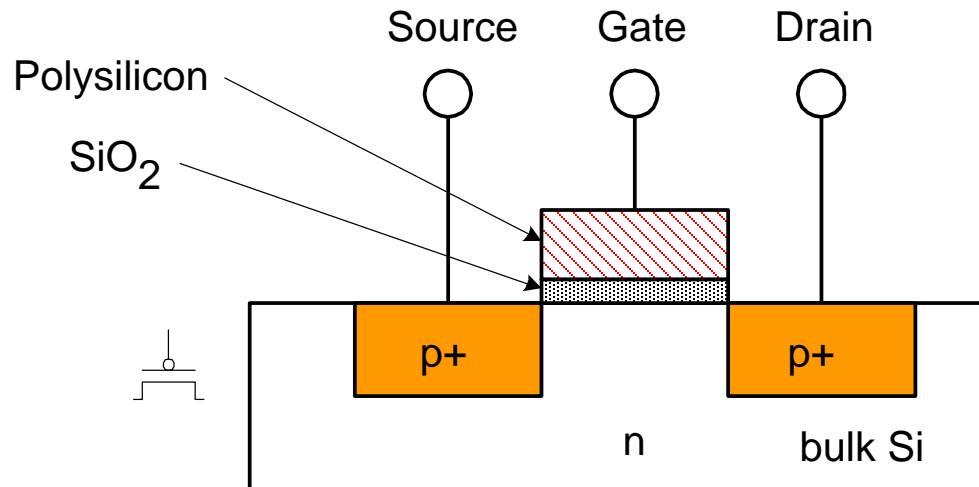
nMOS Operation Cont.

- When the gate is at a high voltage:
 - Positive charge on gate of MOS capacitor
 - Negative charge attracted to body
 - Inverts a channel under gate to n-type
 - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



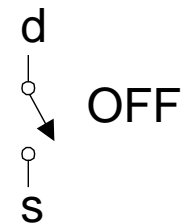
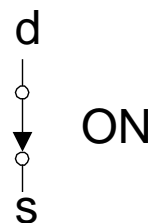
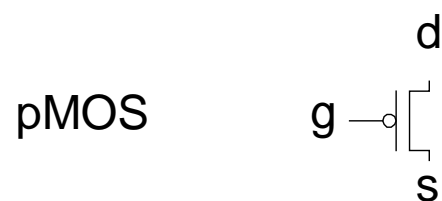
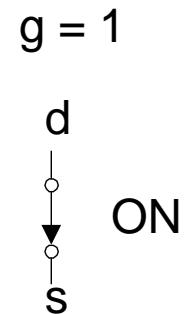
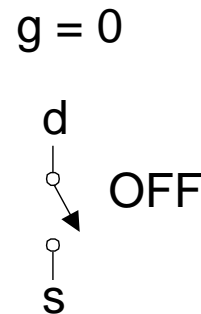
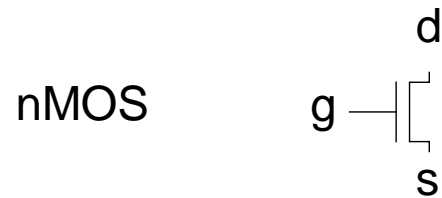
pMOS Transistor

- ❑ Similar, but doping and voltages reversed
 - Body tied to high voltage (V_{DD})
 - Gate low: transistor ON
 - Gate high: transistor OFF
 - Bubble indicates inverted behavior



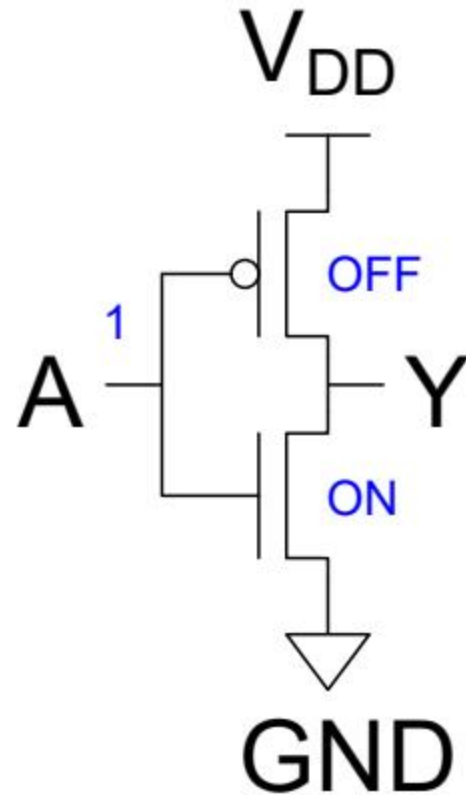
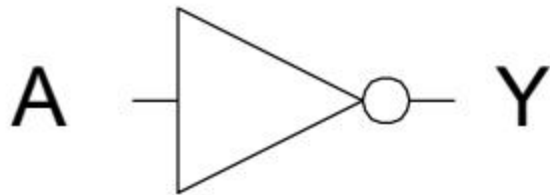
Transistors as Switches

- ❑ We can view MOS transistors as electrically controlled switches
- ❑ Voltage at gate controls path from source to drain



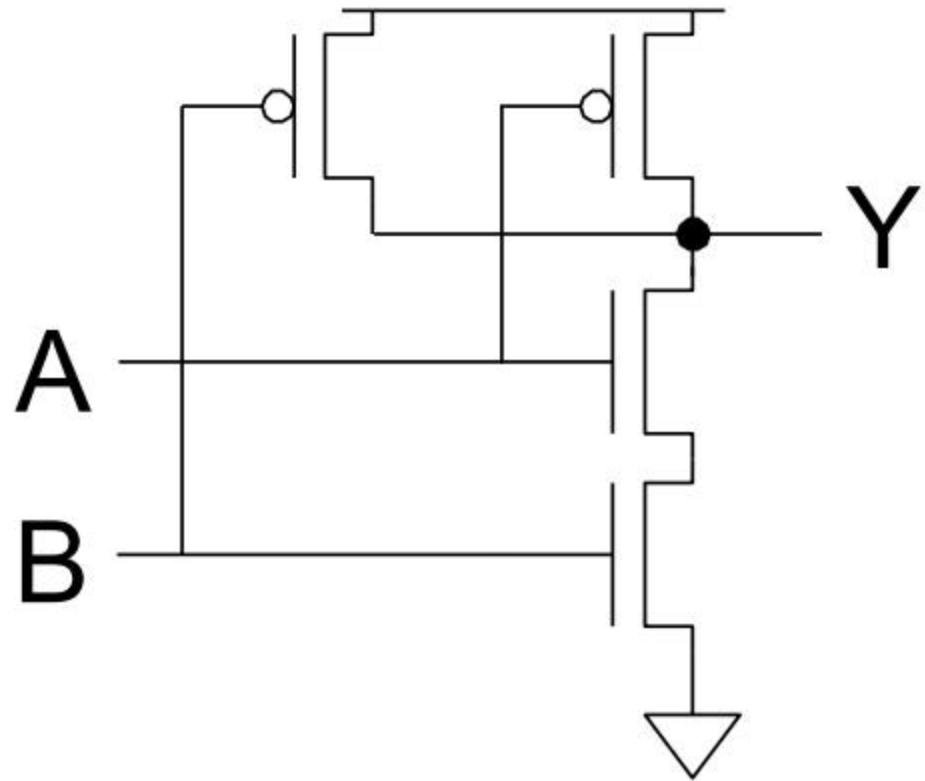
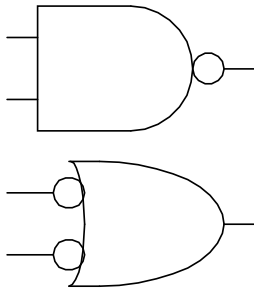
CMOS Inverter

A	Y
0	1
1	0



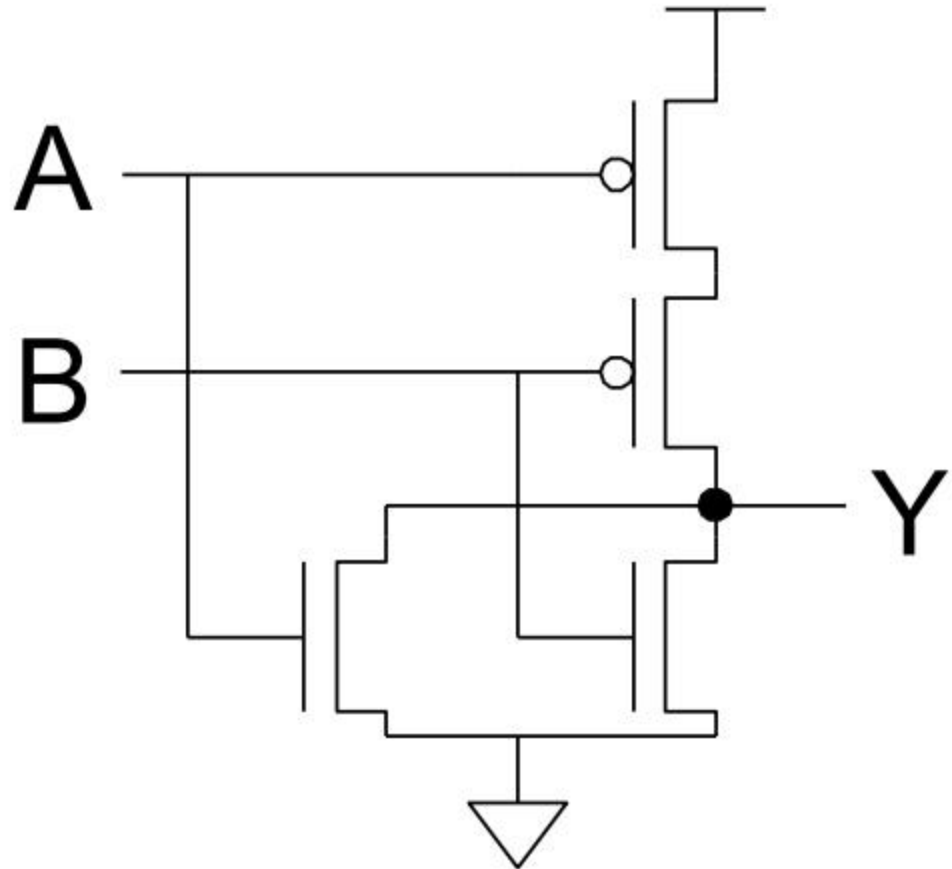
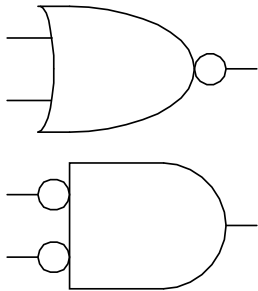
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



CMOS NOR Gate

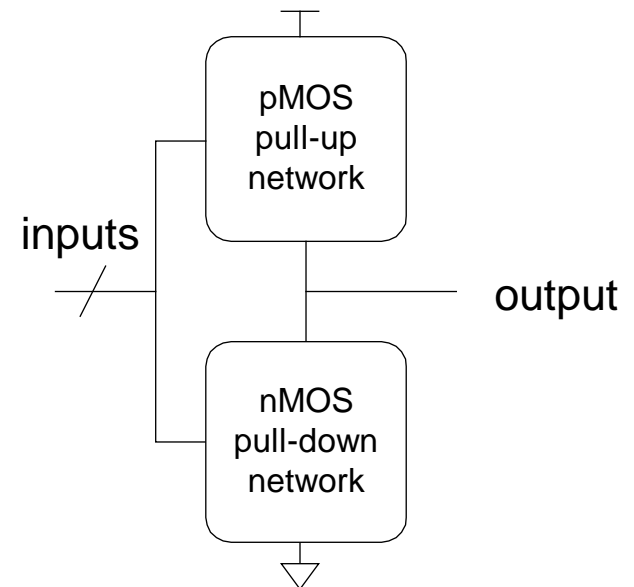
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Complementary CMOS

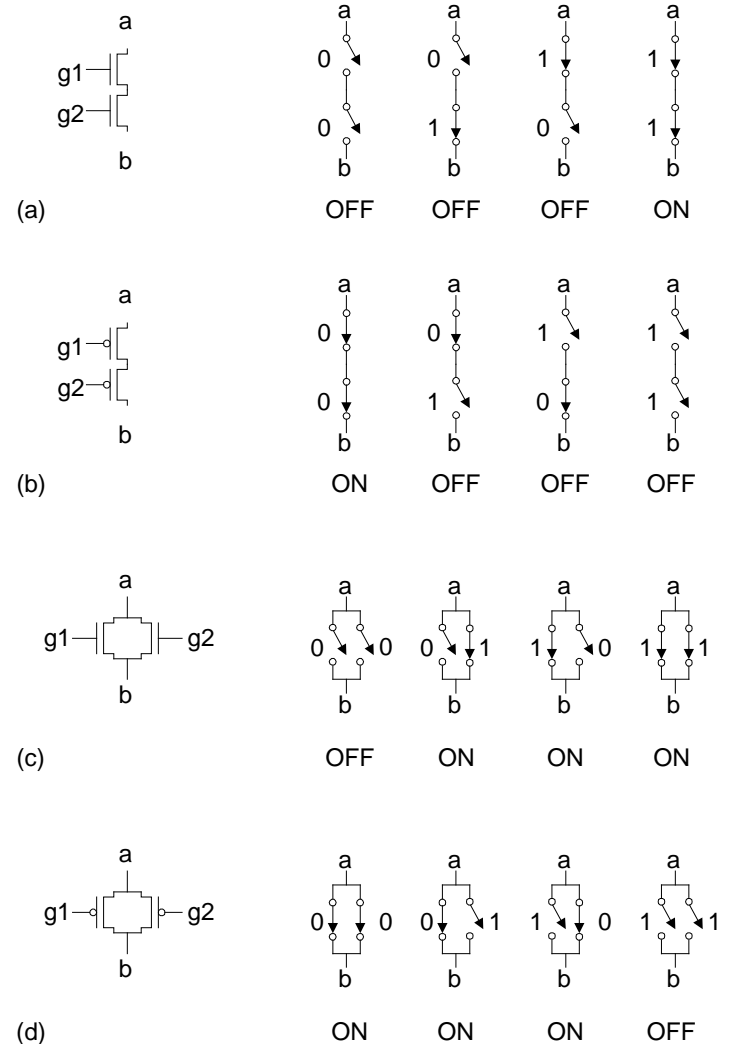
- ❑ Complementary CMOS logic gates
 - nMOS *pull-down network*
 - pMOS *pull-up network*
 - a.k.a. (also known as) static CMOS

	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)



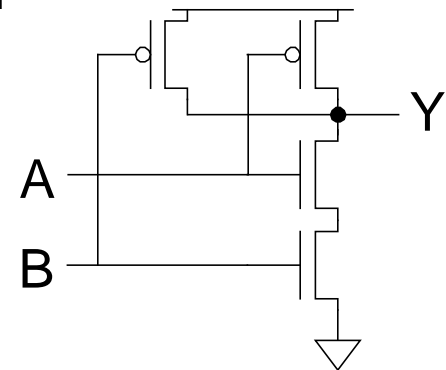
Series and Parallel

- ❑ nMOS: 1 = ON
- ❑ pMOS: 0 = ON
- ❑ *Series*: both must be ON
- ❑ *Parallel*: either can be ON



Conduction Complement

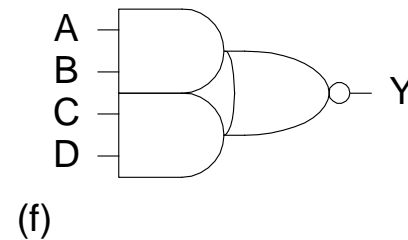
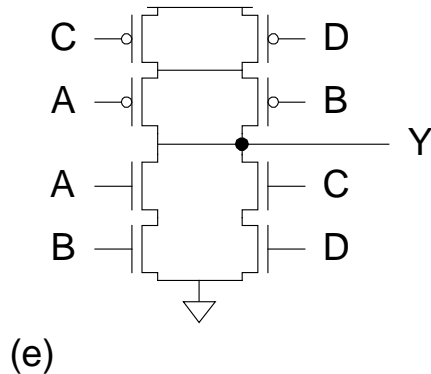
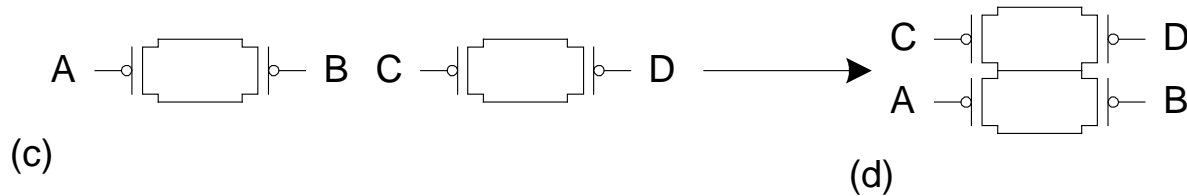
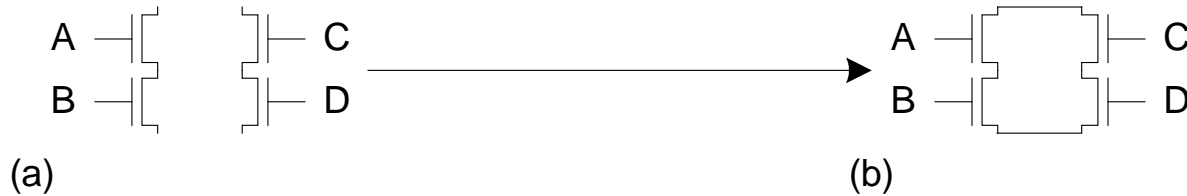
- ❑ Complementary CMOS gates always produce 0 or 1
- ❑ Ex: NAND gate
 - Series nMOS: $Y=0$ when both inputs are 1
 - Thus $Y=1$ when either input is 0
 - Requires parallel pMOS
- ❑ Rule of *Conduction Complements*
 - Pull-up network is complement of pull-down
 - Parallel \rightarrow series, series \rightarrow parallel



Compound Gates

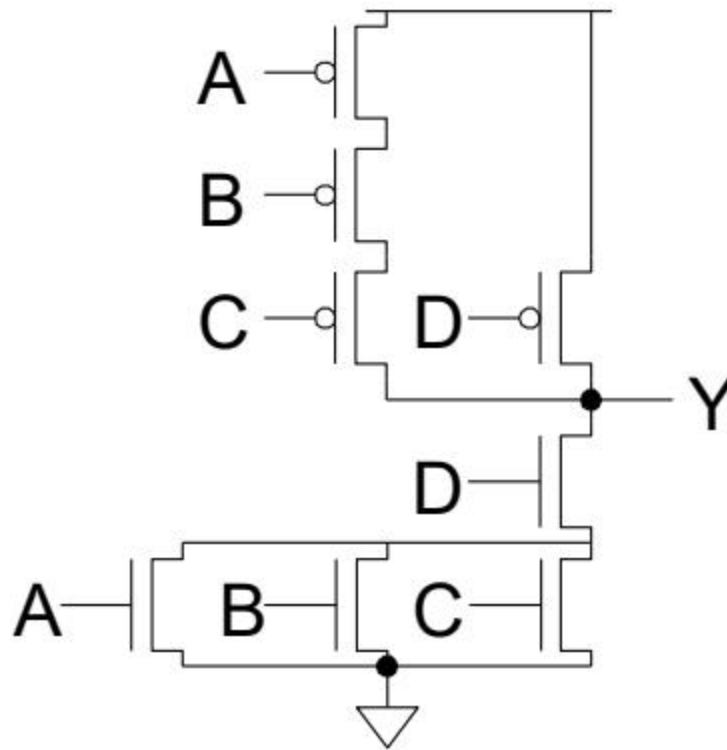
❑ *Compound gates can do any inverting function*

❑ Ex: $Y = \overline{A \cdot B + C \cdot D}$ (AND -OR-INVERT, AOI22)



Example: O3AI

□ $Y = \overline{(A + B + C)} \cdot D$

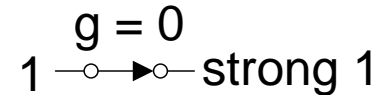
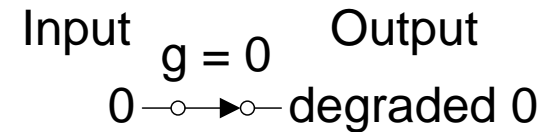
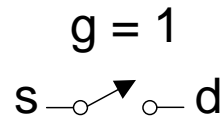
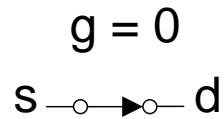
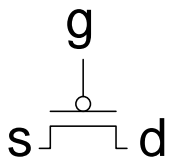
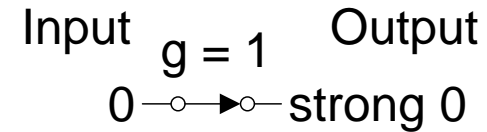
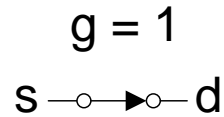
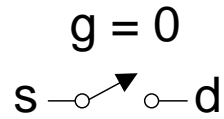
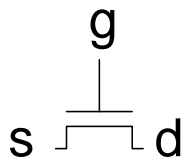


Signal Strength

- ❑ *Strength* of signal
 - How close it approximates ideal voltage source
- ❑ V_{DD} and GND rails are strongest 1 and 0
- ❑ nMOS pass strong 0
 - But degraded or weak 1
- ❑ pMOS pass strong 1
 - But degraded or weak 0
- ❑ Thus nMOS are best for pull-down network

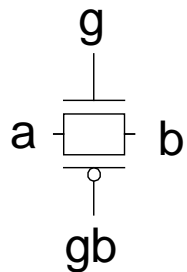
Pass Transistors

- Transistors can be used as switches

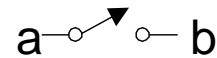


Transmission Gates

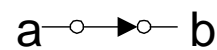
- ❑ Pass transistors produce degraded outputs
- ❑ *Transmission gates* pass both 0 and 1 well



$$g = 0, gb = 1$$



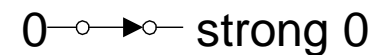
$$g = 1, gb = 0$$



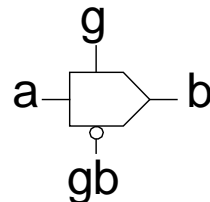
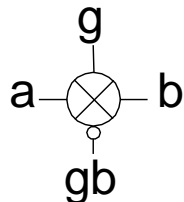
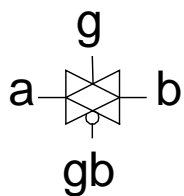
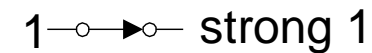
Input

Output

$$g = 1, gb = 0$$



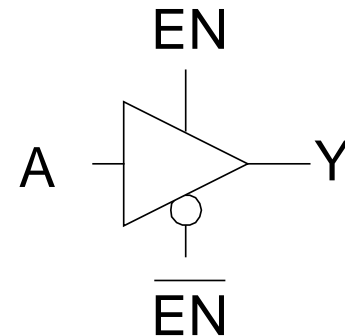
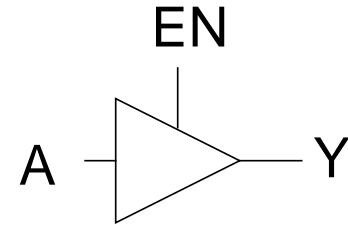
$$g = 1, gb = 0$$



Tristates

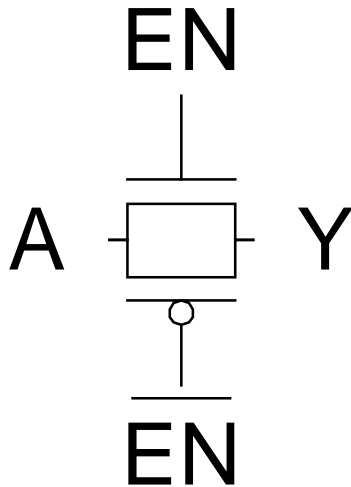
- ❑ *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



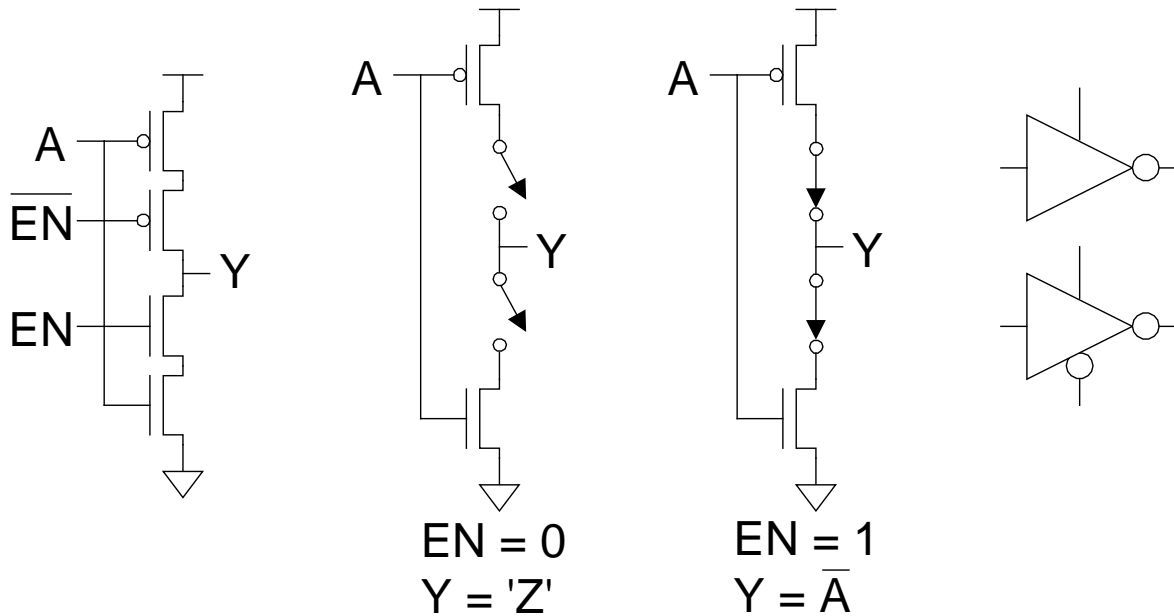
Nonrestoring Tristate

- ❑ Transmission gate acts as tristate buffer
 - Only two transistors
 - But *nonrestoring*
 - Noise on A is passed on to Y



Tristate Inverter

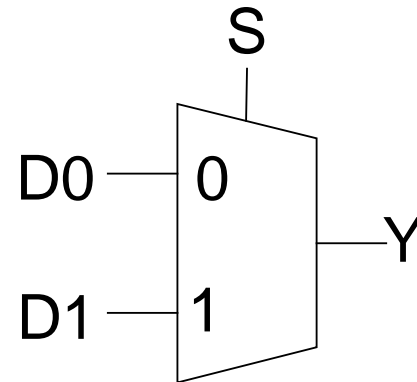
- Tristate inverter produces restored output
 - Violates conduction complement rule
 - Because we want a Z output



Multiplexers

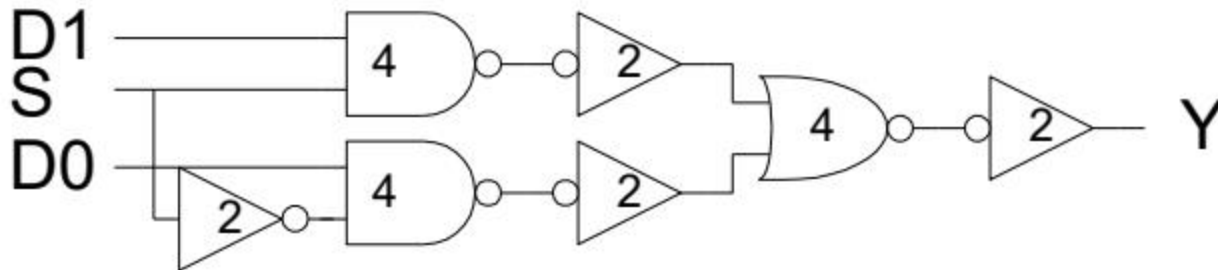
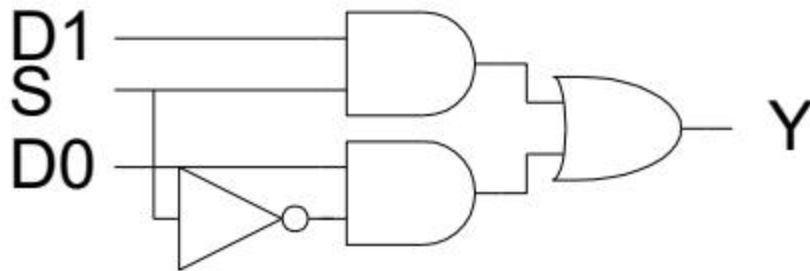
- ❑ 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1



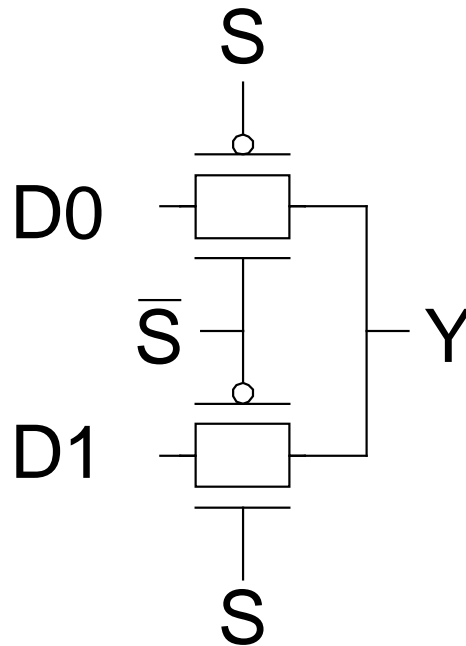
Gate-Level Mux Design

- ❑ $Y = SD_1 + \bar{S}D_0$ (too many transistors)
- ❑ How many transistors are needed?



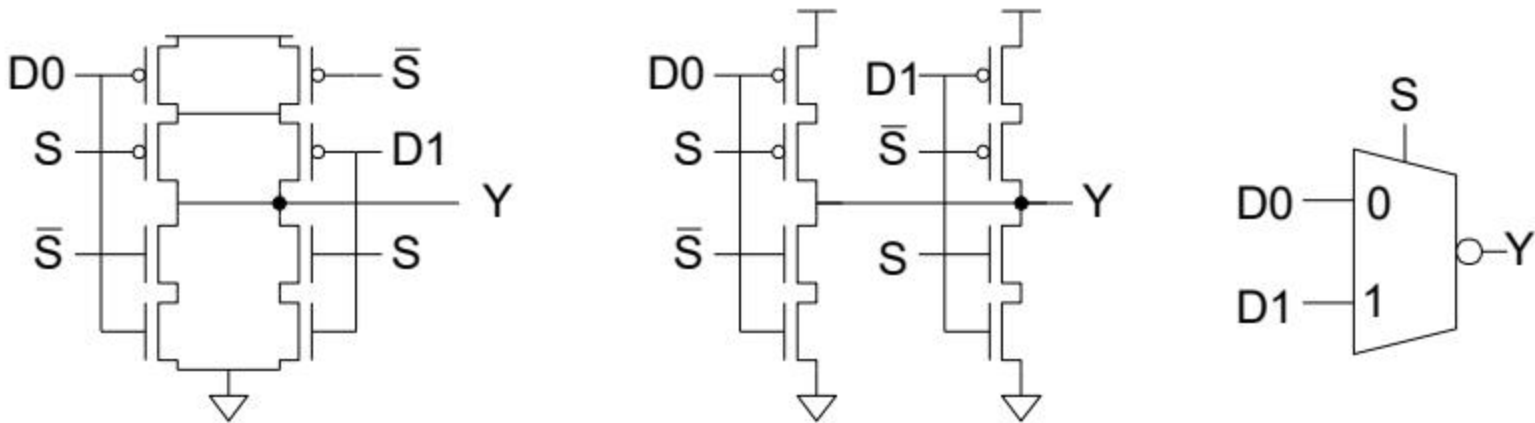
Transmission Gate Mux

- ❑ Nonrestoring mux uses two transmission gates
 - Only 4 transistors



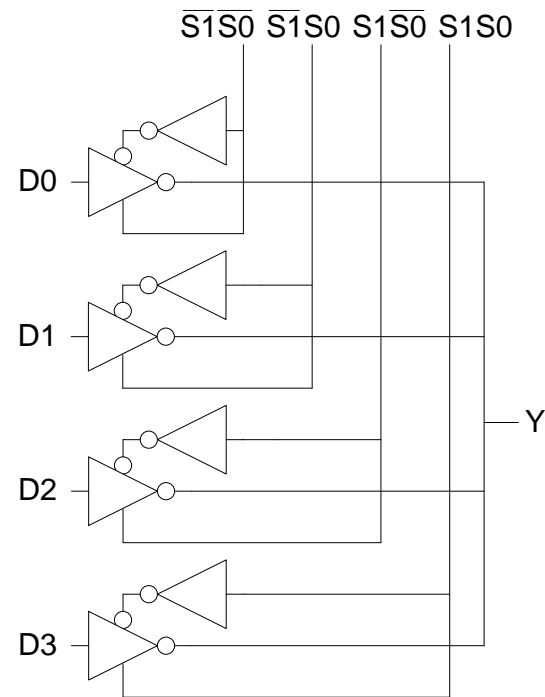
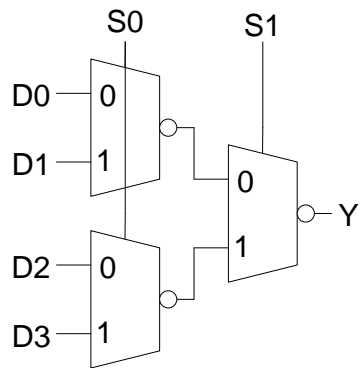
Inverting Mux

- ❑ Inverting multiplexer
 - Use compound AOI22
 - Or pair of tristate inverters
 - Essentially the same thing
- ❑ Noninverting multiplexer adds an inverter



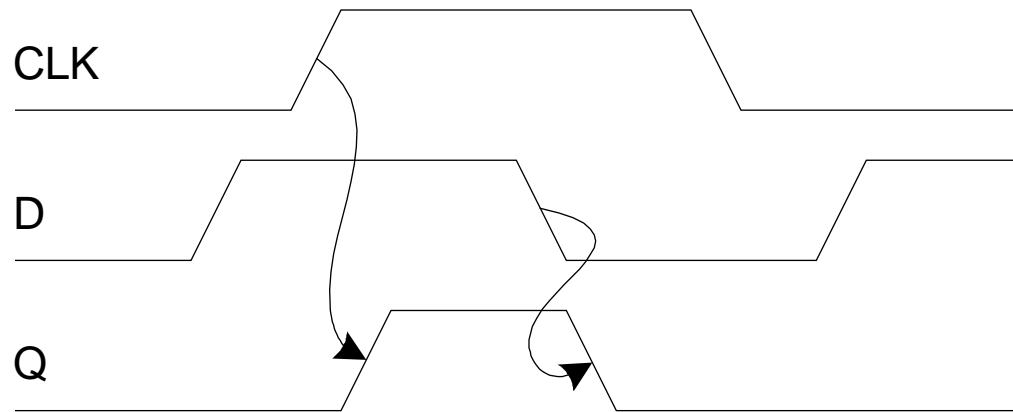
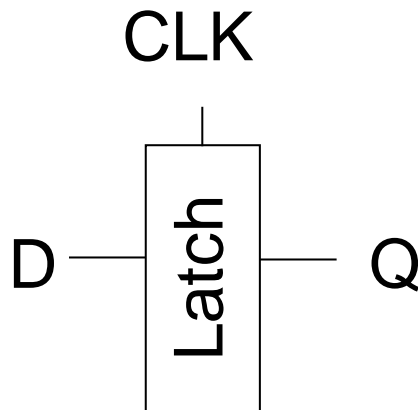
4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
 - Two levels of 2:1 muxes
 - Or four tristates



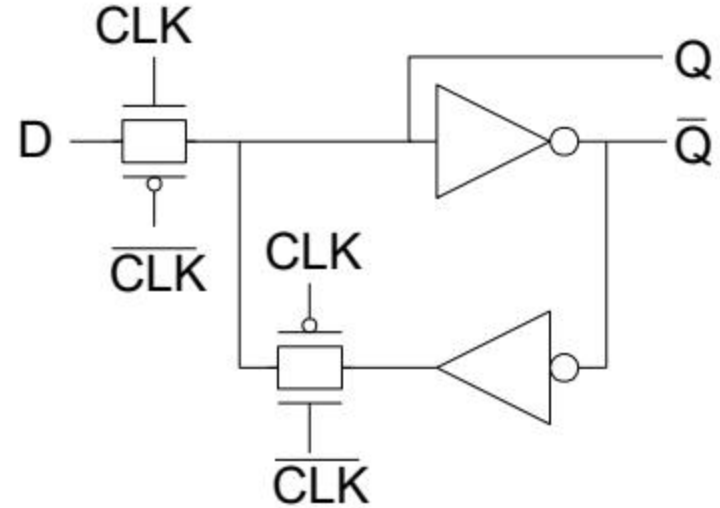
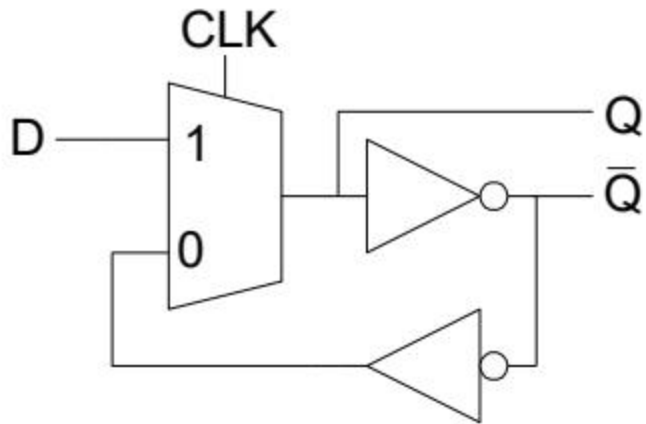
D Latch

- ❑ When $CLK = 1$, latch is *transparent*
 - D flows through to Q like a buffer
- ❑ When $CLK = 0$, the latch is *opaque*
 - Q holds its old value independent of D
- ❑ a.k.a. *transparent latch* or *level-sensitive latch*

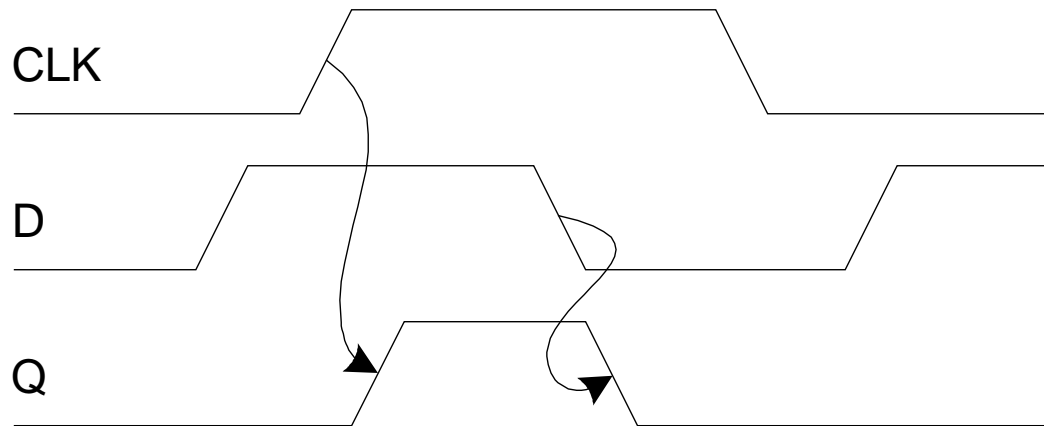
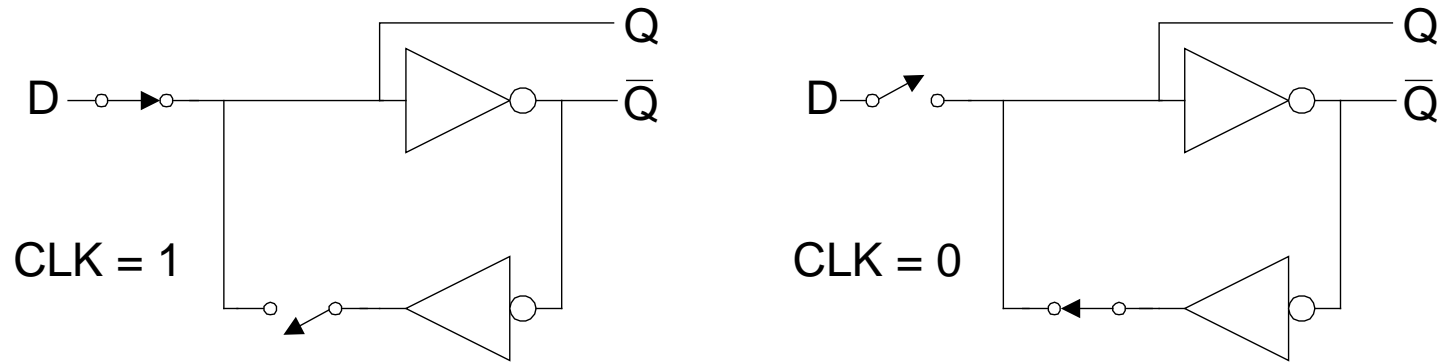


D Latch Design

- ❑ Multiplexer chooses D or old Q

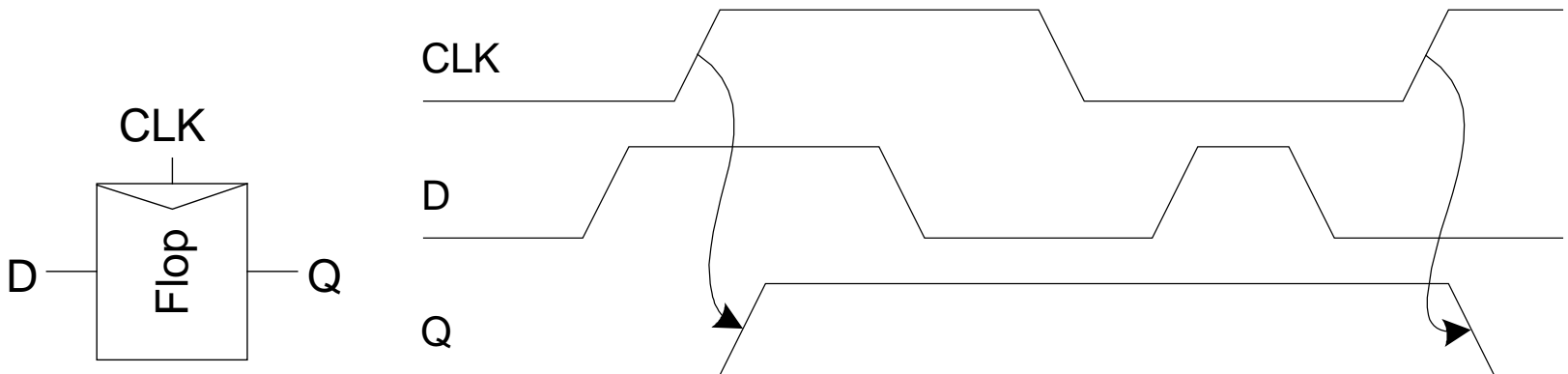


D Latch Operation



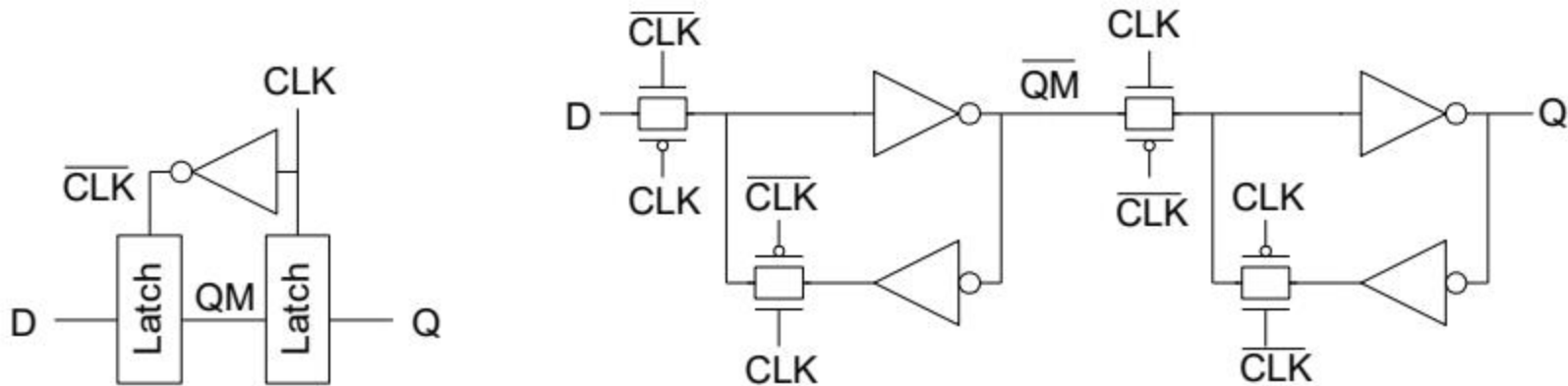
D Flip-flop

- ❑ When CLK rises, D is copied to Q
- ❑ At all other times, Q holds its value
- ❑ a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop*

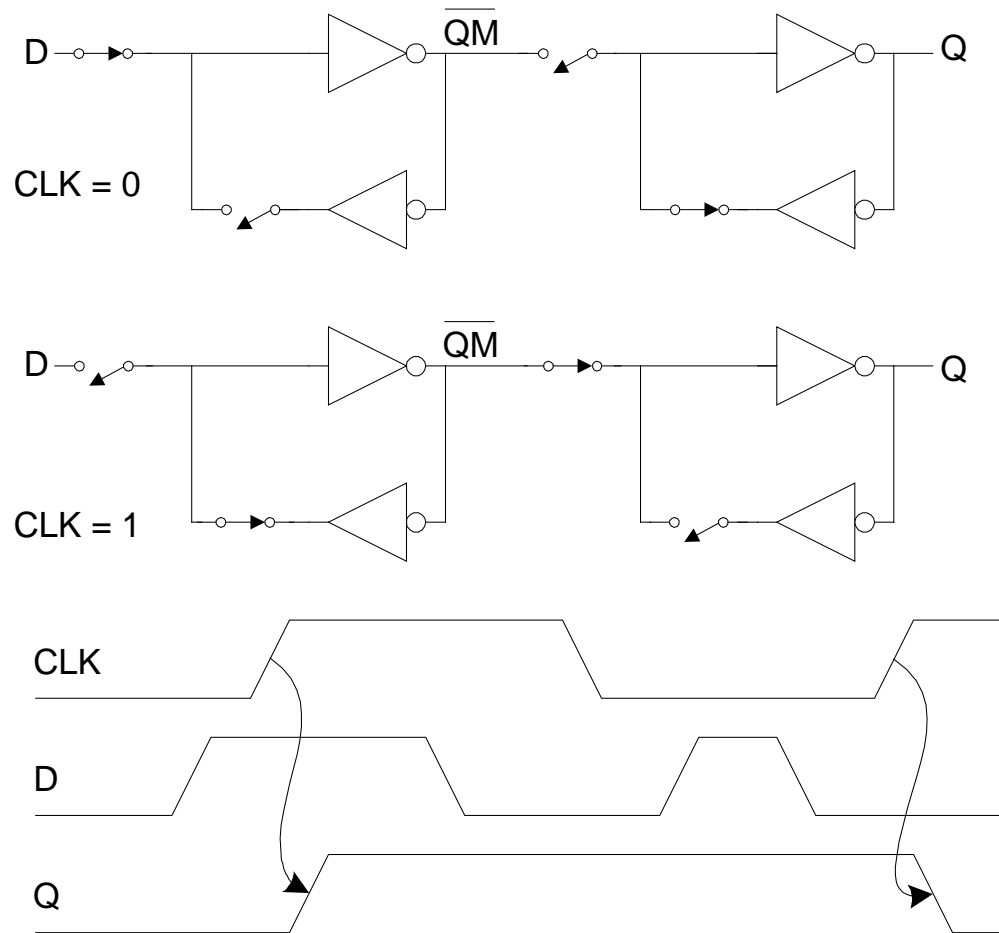


D Flip-flop Design

- Built from master and slave D latches

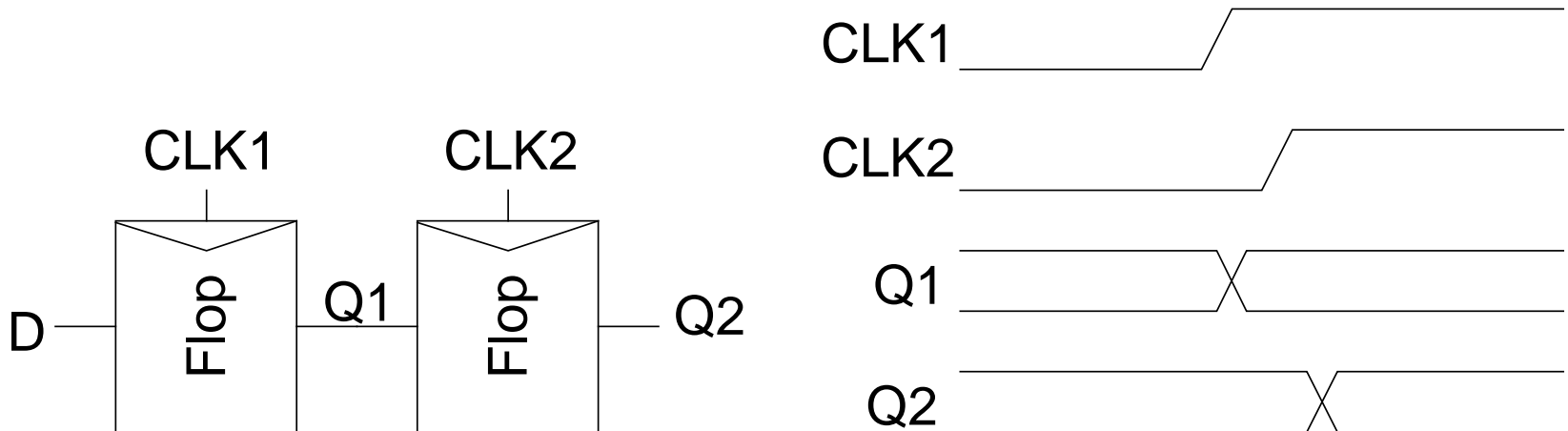


D Flip-flop Operation



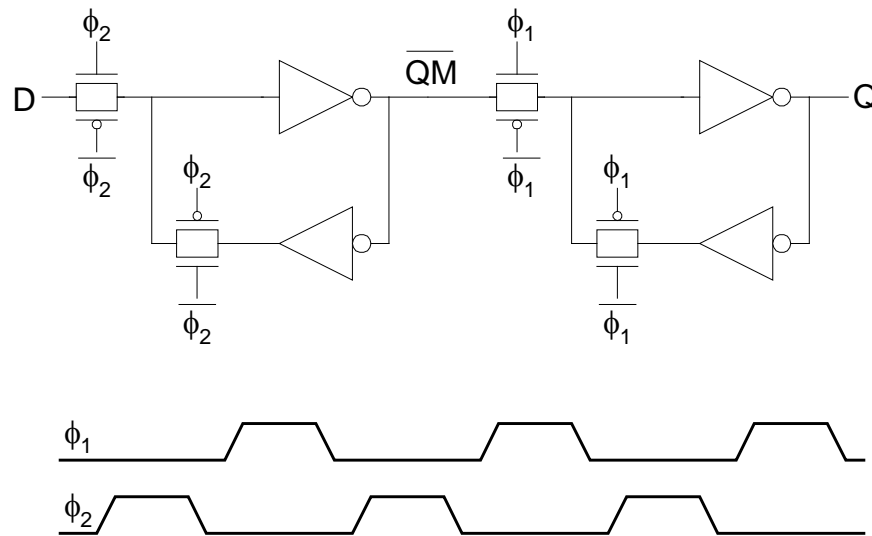
Race Condition

- ❑ Back-to-back flops can malfunction from clock skew
 - Second flip-flop fires late
 - Sees first flip-flop change and captures its result
 - Called *hold-time failure* or *race condition*



Nonoverlapping Clocks

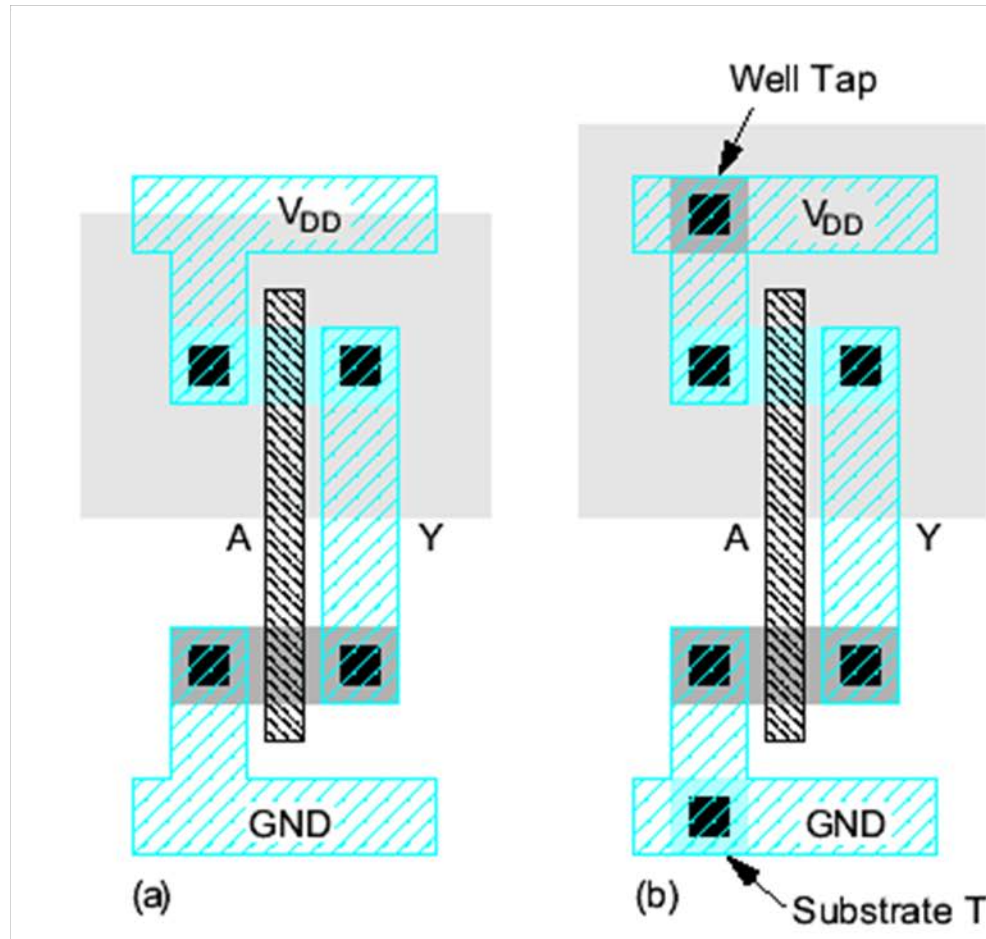
- ❑ Nonoverlapping clocks can prevent races
 - As long as nonoverlap exceeds clock skew
- ❑ We will use them in this class for safe design
 - Industry manages skew more carefully instead



Gate Layout

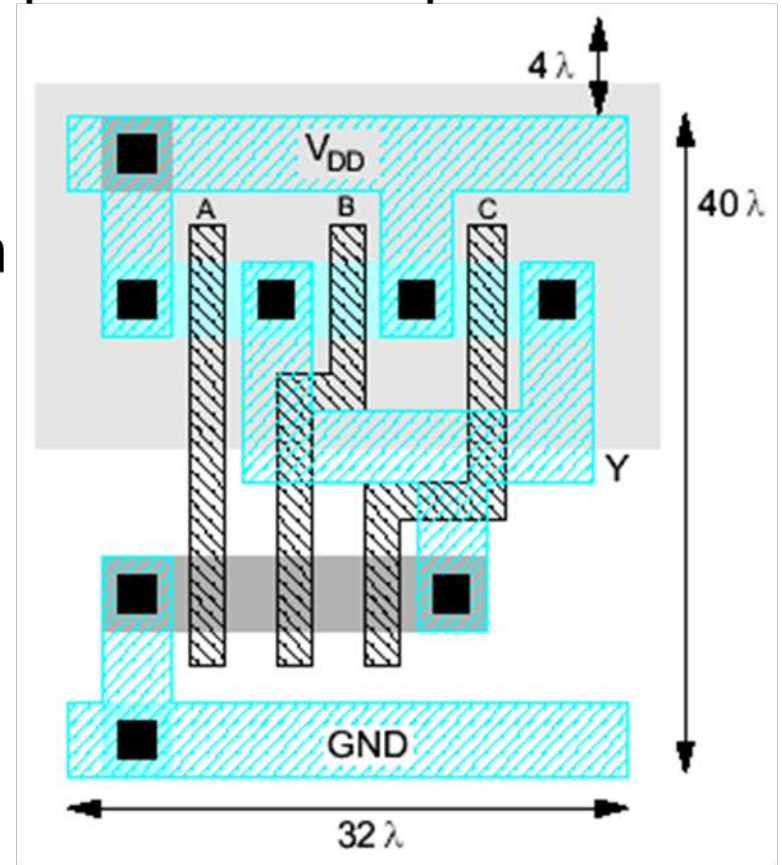
- ❑ Layout can be very time consuming
 - Design gates to fit together nicely
 - Build a library of standard cells
- ❑ Standard cell design methodology
 - V_{DD} and GND should abut (standard height)
 - Adjacent gates should satisfy design rules
 - nMOS at bottom and pMOS at top
 - All gates include well and substrate contacts

Example: Inverter



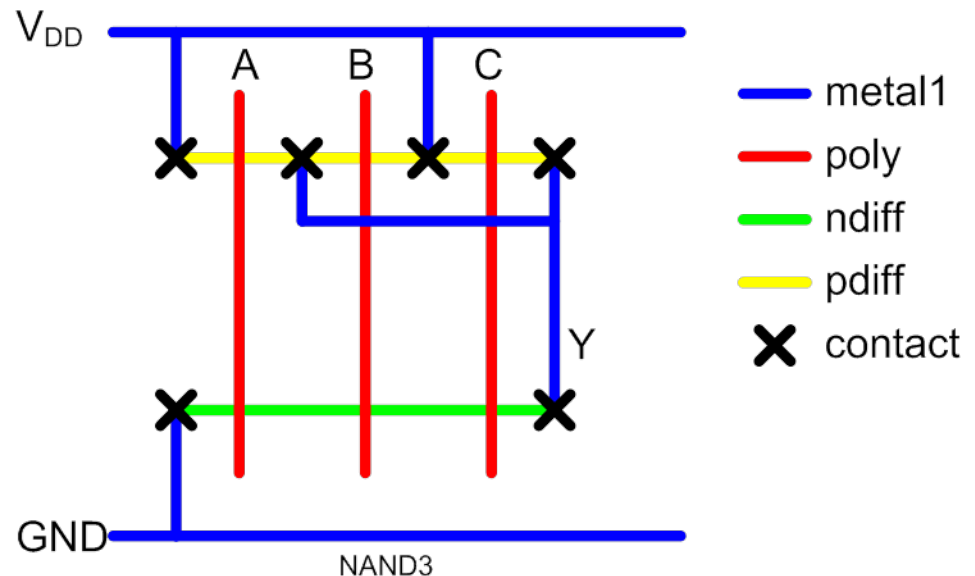
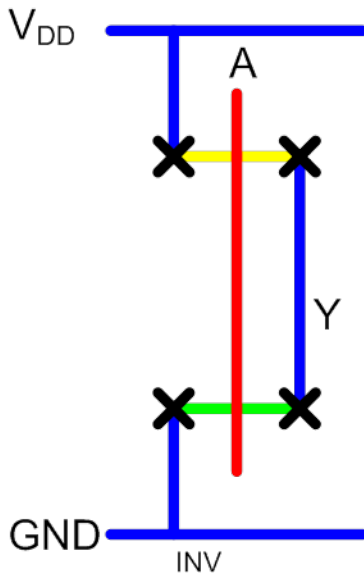
Example: NAND3

- ❑ Horizontal N-diffusion and p-diffusion strips
- ❑ Vertical polysilicon gates
- ❑ Metal1 V_{DD} rail at top
- ❑ Metal1 GND rail at bottom
- ❑ 32λ by 40λ



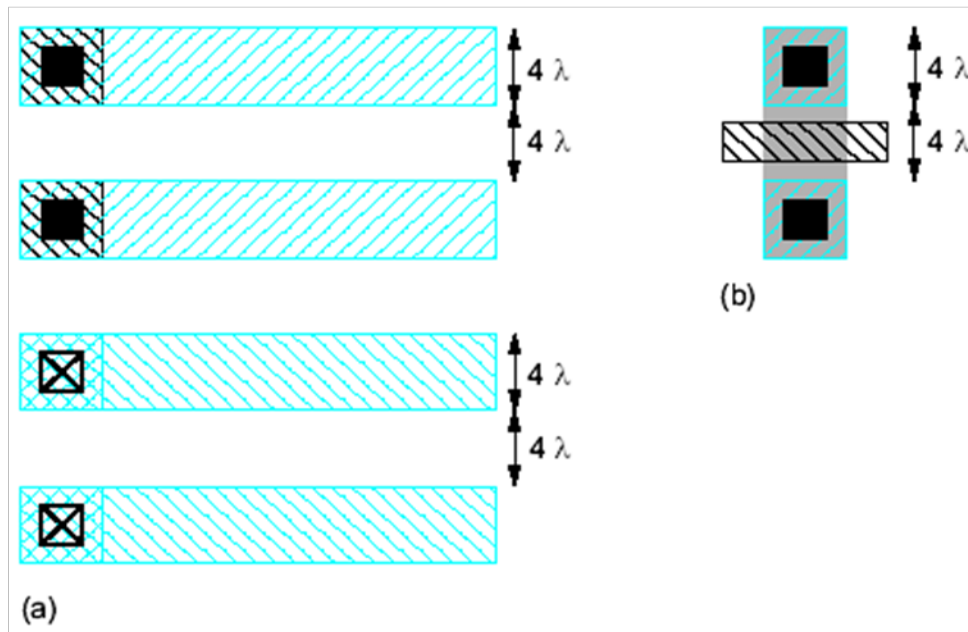
Stick Diagrams

- *Stick diagrams* help plan layout quickly
 - Need not be to scale
 - Draw with color pencils or dry-erase markers



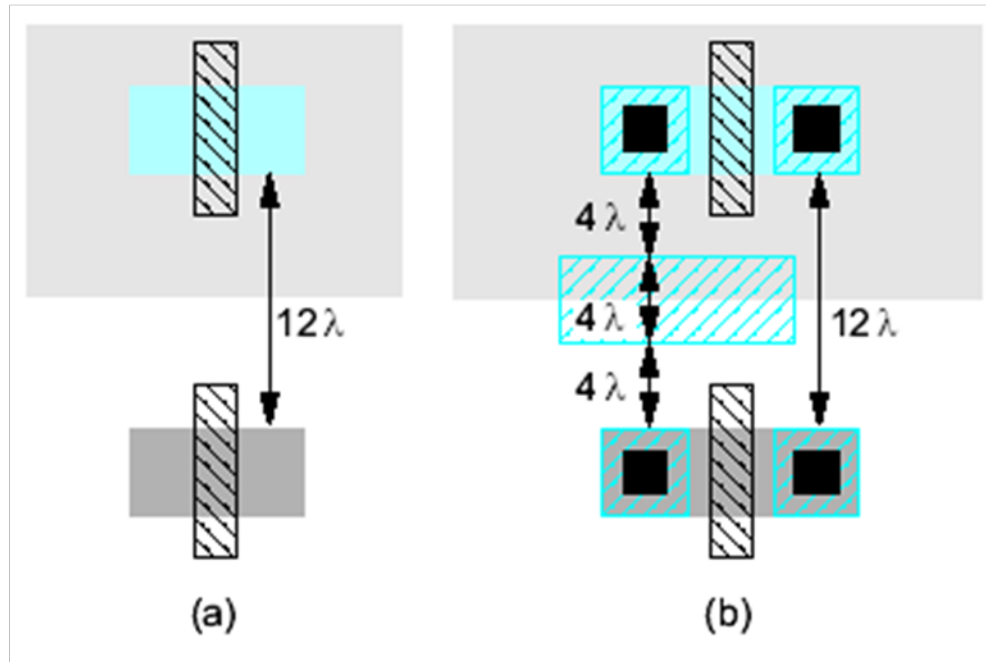
Wiring Tracks

- A *wiring track* is the space required for a wire
 - 4λ width, 4λ spacing from neighbor = 8λ pitch
- Transistors also consume one wiring track



Well spacing

- Wells must surround transistors by 6λ
 - Implies 12λ between opposite transistor flavors
 - Leaves room for one wire track



Summary

- ❑ MOS Transistors (nMOS, pMOS)
- ❑ CMOS Gate Design
(NOR, NAND, Compound, etc...)
- ❑ Pass Transistors
- ❑ CMOS Latches & Flip-Flops
- ❑ Gate Layout