Intergrated Circuits report 1

※ 과제는 A4용지에 자필로 작성한뒤 스테이플러로 제본하여 제출해 주시기 바랍니다.
※ 과제는 Intergrated Circuit Design Fourth Edition 기준으로 출제되었습니다.
시험 당일 중간고사 시작 전 제출

1)
Sketch a transistor-level schematic of a CMOS 3-input XOR gate. You may assume you have both true and complementary versions of the inputs available.
2)
Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions: a) $Y = \overline{ABC + D}$ b) $Y = \overline{(AB + C) \cdot D}$ c) $Y = \overline{AB + C \cdot (A + B)}$
3)
Sketch a stick diagram for a CMOS 4-input NOR gate
4)
Consider the nMOS transistor in a 0.6 μm process with gate oxide thickness of 100 Å. The doping level is $N_A = 2 \times 10^{17}$ cm^{-3} and the nominal threshold voltage is 0.7 V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4 V instead of 0?
5)
A novel inverter has the transfer characteristics shown in Figure 2.34. What are the values of V_{IL}, V_{IH}, V_{OL}, and V_{OH} that give best noise margins? What are these high and low noise margins?

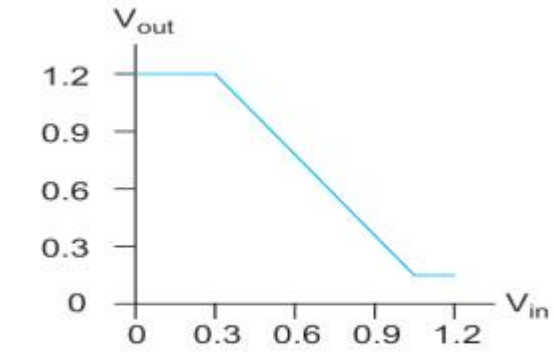


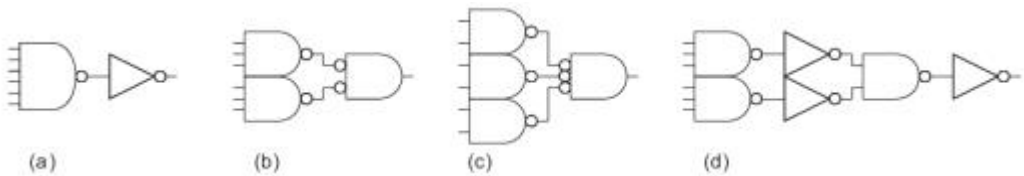
FIGURE 2.34
Transfer characteristics

6)

Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. Compute the rising and falling propagation delays of the NOR gate driving h identical NOR gates using the Elmore delay model. Assume that every source or drain has fully contacted diffusion when making your estimate of capacitance.

7)

Consider four designs of a 6-input AND gate shown in Figure 4.40. Develop an expression for the delay of each path if the path electrical effort is H. What design is fastest for $H = 1$? For $H = 5$? For $H = 20$? Explain your conclusions intuitively.



Ask for answers and fill in the table below.

Design	G	P	N	D (H=1)	D (H=5)	D (H=20)
(a)						
(b)						
(c)						
(d)						

8)

Some designers define a "gate delay" to be a fanout-of-3 2-input NAND gate rather than a fanout-of-4 inverter. Using Logical Effort, estimate the delay of a fanout-of-3 2-input NAND gate. Express your result both in τ and in FO4 inverter delays, assuming $p_{inv} = 1$.

9)

Sketch a 4-input NAND gate with transistor widths chosen to achieve equal rise and fall resistance as a unit inverter. Show why the logical effort is 6/3.