Intergrated Circuits report 1

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1)

Sketch a transistor-level schematic of a CMOS 3-input XOR gate. You may assume you have both true and complementary versions of the inputs available.

2)

Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

a) $Y = \overline{ABC + D}$

b) $Y = \overline{(AB + C) \cdot D}$

c) $Y = \overline{AB + C \cdot (A + B)}$

3)

Sketch a stick diagram for a CMOS 4-input NOR gate

4)

Consider the nMOS transistor in a 0.6 μm process with gate oxide thickness of 100 Å. The doping level is $N_A = 2 \times 10^{17}$ cm^{-3} and the nominal threshold voltage is 0.7 V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4 V instead of 0?

5)

A novel inverter has the transfer characteristics shown in Figure 2.34. What are the values of V_{IL}, V_{IH}, V_{OL}, and V_{OH} that give best noise margins? What are these high and low noise margins?

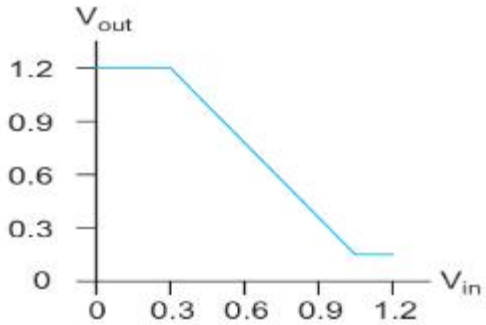

FIGURE 2.34
Transfer characteristics

6)

2.21 Suppose $V_{DD} = 1.2$ V and $V_t = 0.4$ V. Determine V_{out} in Figure 2.36 for the following. Neglect the body effect.

a) $V_{in} = 0$ V

b) $V_{in} = 0.6$ V

c) $V_{in} = 0.9$ V

d) $V_{in} = 1.2$ V.

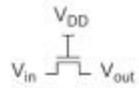

FIGURE 2.36
Single pass transistor

7)

A 90 nm long transistor has a gate oxide thickness of 16 Å. What is its gate capacitance per micron of width?

8)

Sketch a 2-input NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter. Compute the rising and falling propagation delays of the NOR gate driving h identical NOR gates using the Elmore delay model. Assume that every source or drain has fully contacted diffusion when making your estimate of capacitance.

9)

Estimate worst-case rising and falling delay of 3-input NAND driving h identical gates.