Digital engineering 3st report

디지털 공학 과제 주의사항

과제는 반드시 **자필**로 작성하셔야 합니다.
문제 풀이 과정이 다 들어가 있어야 하며, 제출 기한은 5월 19일 입니다,
A4용지에 반드시 풀이과정과 학번 이름을 포함하여 11시~13시까지 ICAT 연구실 과제 제출함에 제출해주시기 바랍니다. (늦게 제출 시 페널티 감점 있습니다.)
문제는 7판 원서 기준으로 출제되었습니다.

7.2 Realize the following functions using AND and OR gates. Assume that there are no restrictions on the number of gates which can be cascaded and minimize the number of gate inputs.

(a) $AC'D + ADE' + BE' + BC' + A'D'E'$

(b) $AE + BDE + BCE + BCFG + BDFG + AFG$

7.10 Find a minimum two-level, multiple-output AND-OR gate circuit to realize these functions.

$$f_1(a, b, c, d) = \Sigma\, m(3, 4, 6, 9, 11)$$
$$f_2(a, b, c, d) = \Sigma\, m(2, 4, 8, 10, 11, 12)$$
$$f_3(a, b, c, d) = \Sigma\, m(3, 6, 7, 10, 11) \qquad \text{(11 gates minimum)}$$

7.15 Using AND and OR gates, find a minimum two-level circuit to realize

(a) $F = a'c + bc'd + ac'd$

(b) $F = (b' + c)(a + b' + d)(a + b + c' + d)$

(c) $F = a'cd' + a'bc + ad$

(d) $F = a'b + ac + bc + bd'$

7.21 Realize each of the following functions as a minimum two-level NAND-gate circuit and as a minimum two-level NOR-gate circuit.

(a) $F(A,B,C,D) = BD' + B'CD + A'BC + A'BC'D + B'D'$

(b) $f(a, b, c, d) = \Pi\, M(0, 1, 7, 9, 10, 13) \cdot \Pi\, D(2, 6, 14, 15)$

(c) $f(a, b, c, d) = \Sigma\, m(0, 2, 5, 10) + \Sigma\, d(3, 6, 9, 13, 14, 15)$

(d) $F(A, B, C, D, E) = \Sigma\, m(0, 2, 4, 5, 11, 14, 16, 17, 18, 22, 23, 25, 26, 31) + \Sigma\, d(3, 19, 20, 27, 28)$

(e) $F(A, B, C, D, E) = \Pi\, M(3, 4, 8, 9, 10, 11, 12, 13, 14, 16, 19, 22, 25, 27) \cdot \Pi\, D(17, 18, 28, 29)$

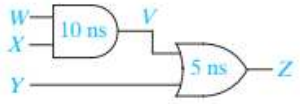
(f) $f(a, b, c, d) = \Pi\, M(1, 3, 10, 11, 13, 14, 15) \cdot \Pi\, D(4, 6)$

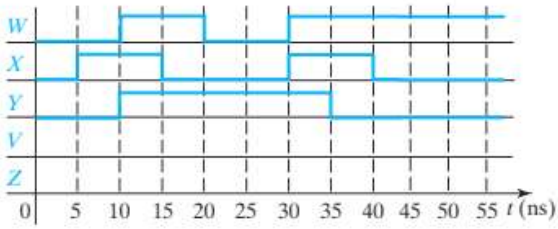
(g) $f(w, x, y, z) = \Sigma\, m(1, 2, 4, 6, 8, 9, 11, 12, 13) + \Sigma\, d(0, 7, 10, 15)$

7.41 In which of the following two-level circuit forms can an arbitrary switching function be realized? Verify your answers. (Assume the inputs are available in both complemented and uncomplemented form.)

(a) NOR-AND
(b) NOR-OR
(c) NOR-NAND
(d) NOR-XOR
(e) NAND-AND
(f) NAND-OR
(g) NAND-NOR
(h) NAND-XOR

8.10 Draw the timing diagram for V and Z for the circuit. Assume that the AND gate has a delay of 10 ns and the OR gate has a delay of 5 ns.

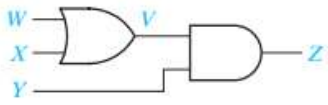


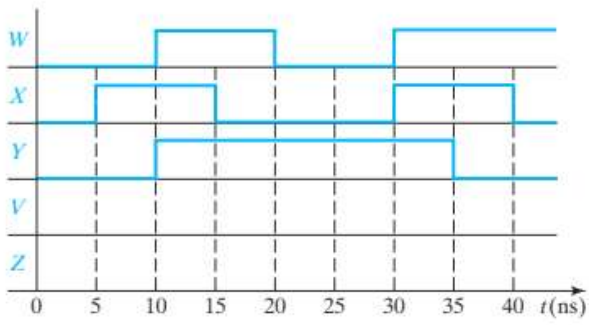


8.11 Consider the three-level circuit corresponding to the expression $f(A, B, C, D) = (A + B)(B'C' + BD')$.

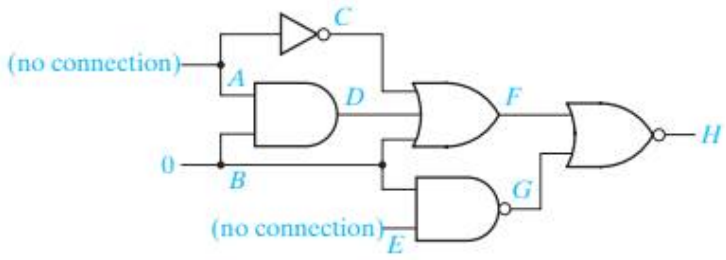
(a) Find all hazards in this circuit.
(b) Redesign the circuit as a three-level NOR circuit that is free of all hazards.

8.12 Complete the timing diagram for the given circuit. Assume that both gates have a propagation delay of 5 ns.





8.14 Using four-valued logic, find A, B, C, D, E, F, G, and H.



8.16 Consider the following logic function.

$$F(A, B, C, D) = \Sigma\, m(0, 2, 5, 6, 7, 8, 9, 12, 13, 15)$$

(a) Find two different minimum AND-OR circuits which implement F. Identify two hazards in each circuit. Then find an AND-OR circuit for F that has no hazards.
(b) The minimum OR-AND circuit for F has one hazard. Identify it, and then find an OR-AND circuit for F that has no hazards.

9.1 (a) Show how two 2-to-1 multiplexers (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows:
If $AB = 00$, select I_0
If $AB = 01$, select I_1
If $AB = 1-$ (B is a don't-care), select I_2
(b) Show how two 4-to-1 and one 2-to-1 multiplexers could be connected to form an 8-to-1 MUX with three control inputs.
(c) Show how four 2-to-1 and one 4-to-1 multiplexers could be connected to form an 8-to-1 MUX with three control inputs.

9.7 An adder for Gray-coded-decimal digits (see Table 1-2) is to be designed using a ROM. The adder should add two Gray-coded digits and give the Gray-coded sum and a carry. For example, 1011 + 1010 = 0010 with a carry of 1 (7 + 6 = 13). Draw a block diagram showing the required ROM inputs and outputs. What size ROM is required? Indicate how the truth table for the ROM would be specified by giving some typical rows.

9.20 Realize the function $f(a, b, c, d, e) = \Sigma\, m(6, 7, 9, 11, 12, 13, 16, 17, 18, 20, 21, 23, 25, 28)$ using a 16-to-1 MUX with control inputs b, c, d, and e. Each data input should be 0, 1, a, or a'. (*Hint:* Start with a minterm expansion of F and combine minterms to eliminate a and a' where possible.)

9.21 Implement a full adder

(a) using two 8-to-1 MUXes. Connect X,Y, and C_{in} to the control inputs of the MUXes and connect 1 or 0 to each data input.

(b) using two 4-to-1 MUXes and one inverter. Connect X and Y to the control inputs of the MUXes, and connect 1's, 0's, C_{in}, or C'_{in} to each data input.

(c) again using two 4-to-1 MUXes, but this time connect C_{in} and Y to the control inputs of the MUXes, and connect 1's, 0's, X, or X' to each data input. Note that in this fashion, any N-variable logic function may be implemented using a $2^{(N-1)}$-to-1 MUX.

9.28 Design an adder for excess-3 decimal digits (see Table 1-2) using a ROM. Add two excess-3 digits and give the excess-3 sum and a carry. For example, 1010 + 1001 = 0110 with a carry of 1 (7 + 6 = 13). Draw a block diagram showing the required ROM inputs and outputs. What size ROM is required? Indicate how the truth table for the ROM would be specified by giving some typical rows.